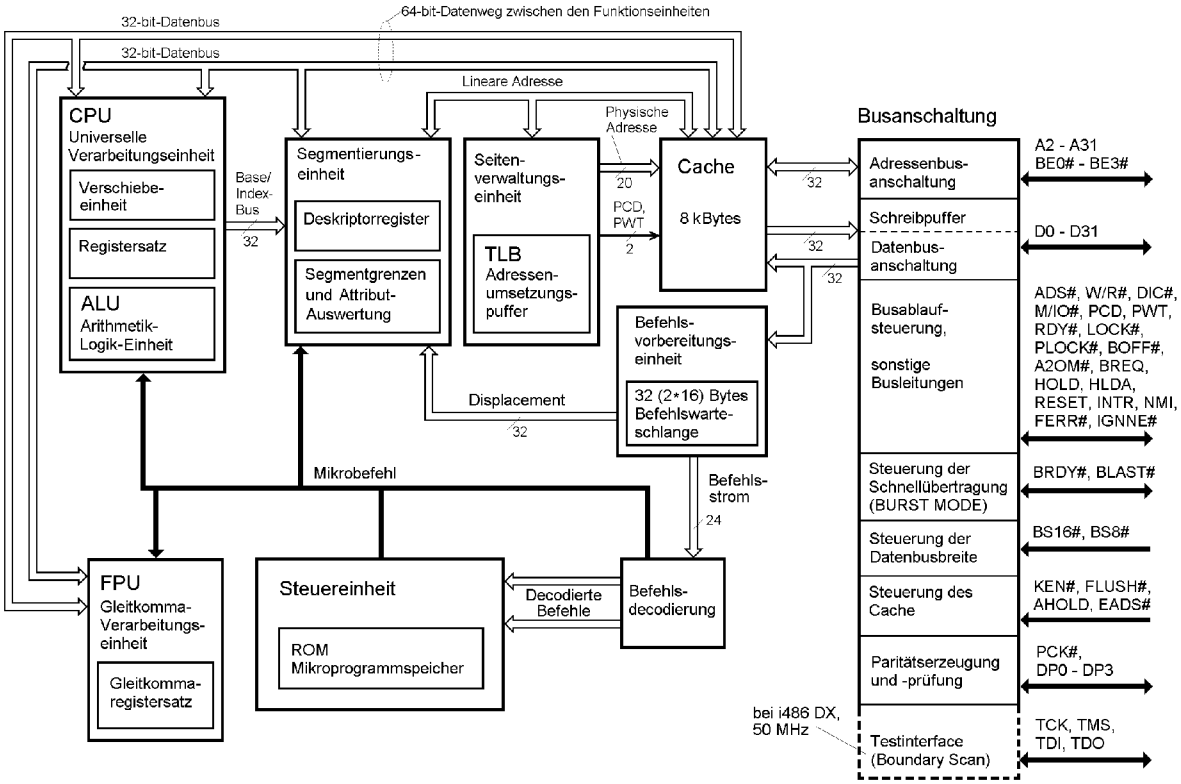
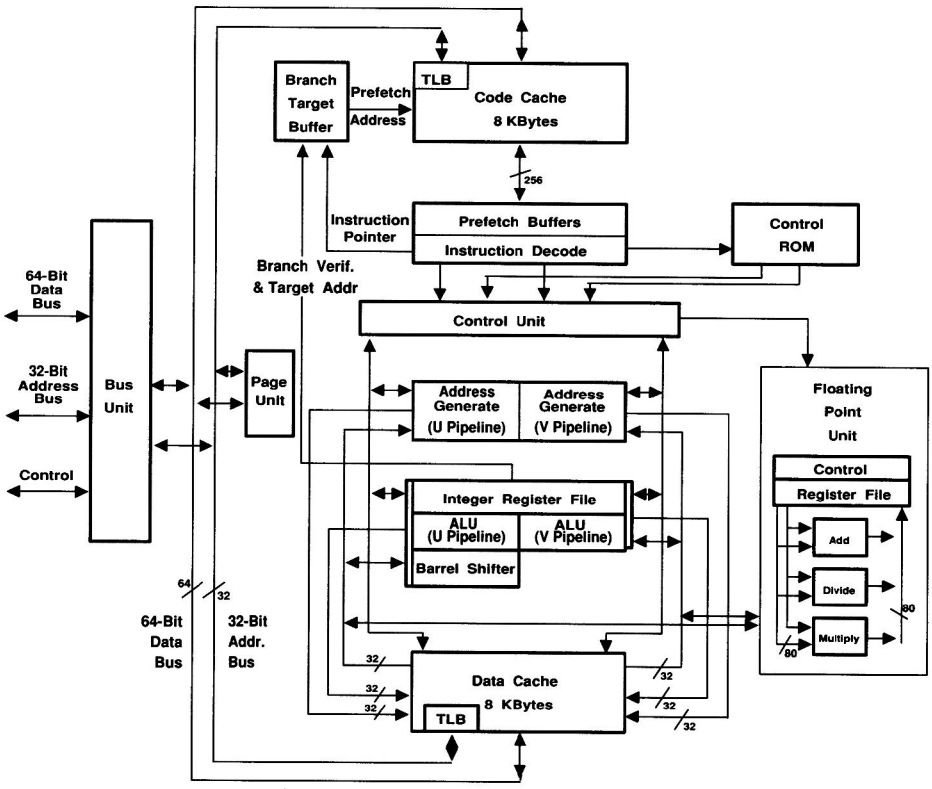
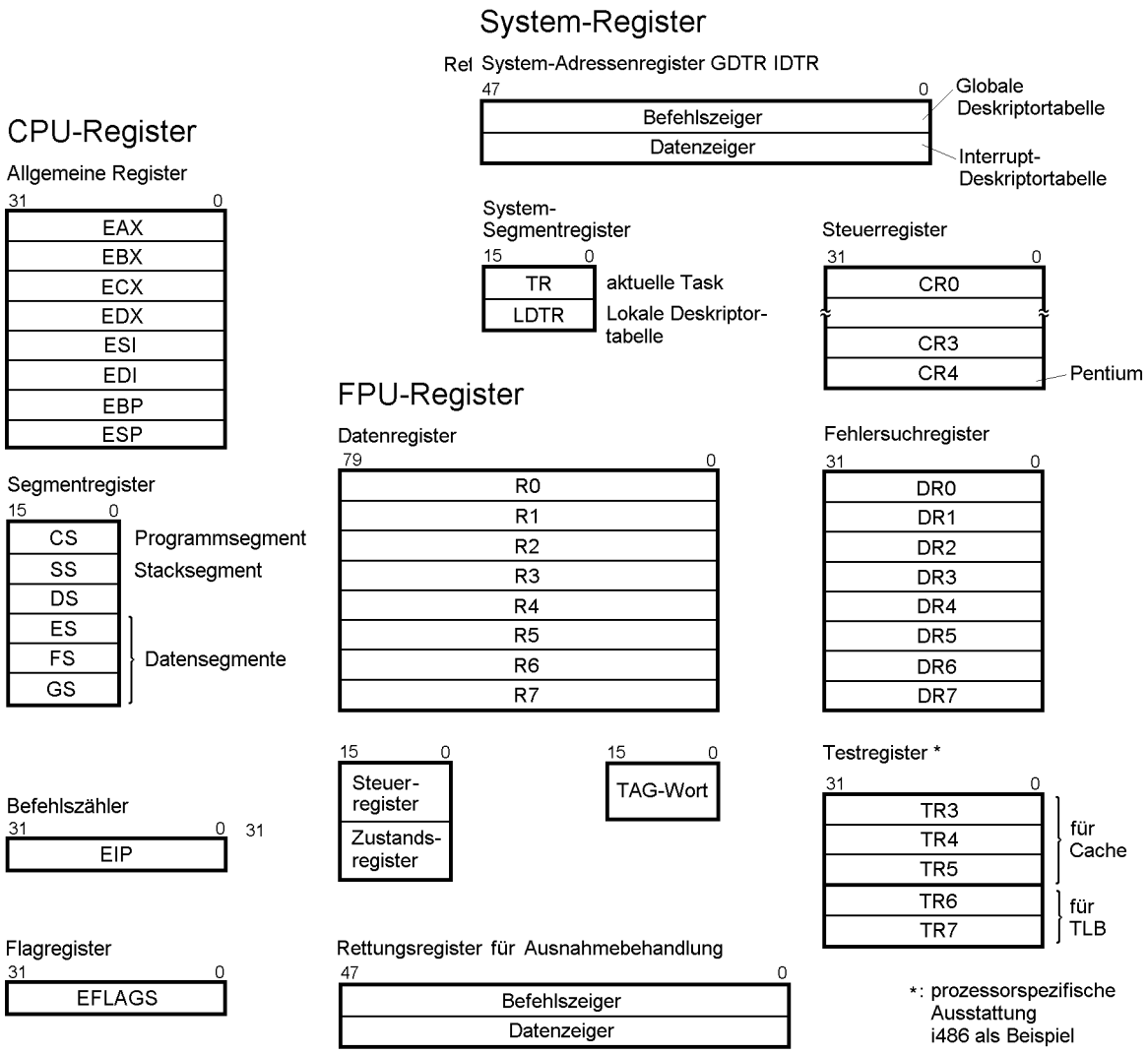
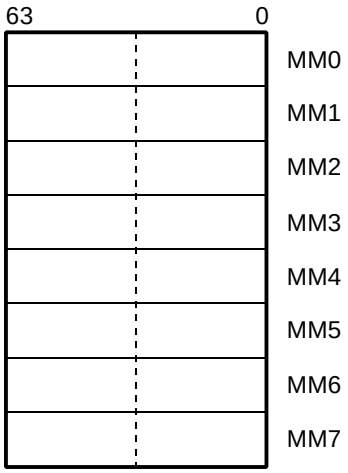

32-bit-Datenbus
64-bit-Datenweg zwischen den Funktionseinheiten
32-bit-Datenbus
Lineare Adresse
Physische Adresse
Busanschaltung
CPU
Universelle Verarbeitungseinheit
Verschiebe-einheit
Registersatz
ALU
Arithmetik-Logik-Einheit
Base/ Index-Bus
32
Segmentierungs-einheit
Deskriptorregister
Segmentgrenzen und Attribut-Auswertung
Seiten-verwaltungs-einheit
TLB
Adressen-umsetzungs-puffer
20
PCD, PWT
2
Cache
8 kBytes
32
32
32
Befehls-vorbereitungs-einheit
32 (2*16) Bytes Befehlswarte-schlange
Displacement
32
Mikrobefehl
Befehls-strom
24
FPU
Gleitkomma-Verarbeitungs-einheit
Gleitkomma-registersatz
Steuereinheit
ROM Mikroprogrammspeicher
Decodierte Befehle
Befehls-decodierung
Adressenbus-anschaltung
Schreibpuffer
Datenbus-anschaltung
Busablauf-steuerung,
sonstige Busleitungen
Steuerung der Schnellübertragung (BURST MODE)
Steuerung der Datenbusbreite
Steuerung des Cache
Paritätserzeugung und -prüfung
Testinterface (Boundary Scan)
A2 - A31
BE0# - BE3#
D0 - D31
ADS#, W/R#, DIC#, M/IO#, PCD, PWT, RDY#, LOCK#, PLOCK#, BOFF#, A20M#, BREQ, HOLD, HLDA, RESET, INTR, NMI, FERR#, IGNNE#
BRDY#, BLAST#
BS16#, BS8#
KEN#, FLUSH#, AHOLD, EADS#
PCK#, DP0 - DP3
TCK, TMS, TDI, TDO
bei i486 DX, 50 MHz

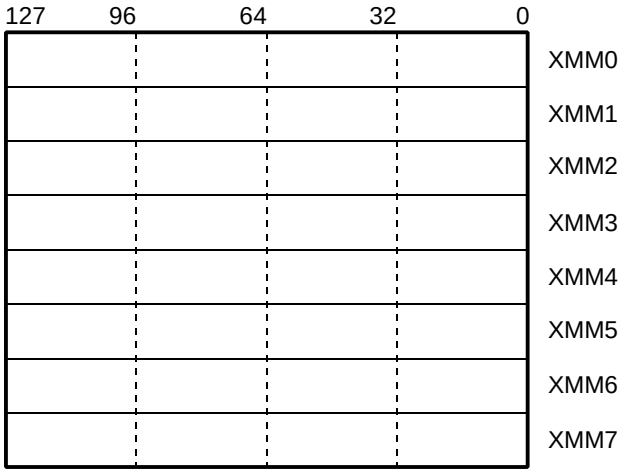

Branch Target Buffer
Prefetch Address
TLB
Code Cache 8 KBytes
256
Instruction Pointer
Prefetch Buffers
Instruction Decode
Control ROM
Branch Verif. & Target Addr
Control Unit
64-Bit Data Bus
32-Bit Address Bus
Control
Bus Unit
Page Unit
Address Generate (U Pipeline)
Address Generate (V Pipeline)
Floating Point Unit
Control
Register File
Integer Register File
ALU (U Pipeline)
ALU (V Pipeline)
Barrel Shifter
Add
Divide
Multiply
80
64
32
64-Bit Data Bus
32-Bit Addr. Bus
Data Cache 8 KBytes
TLB

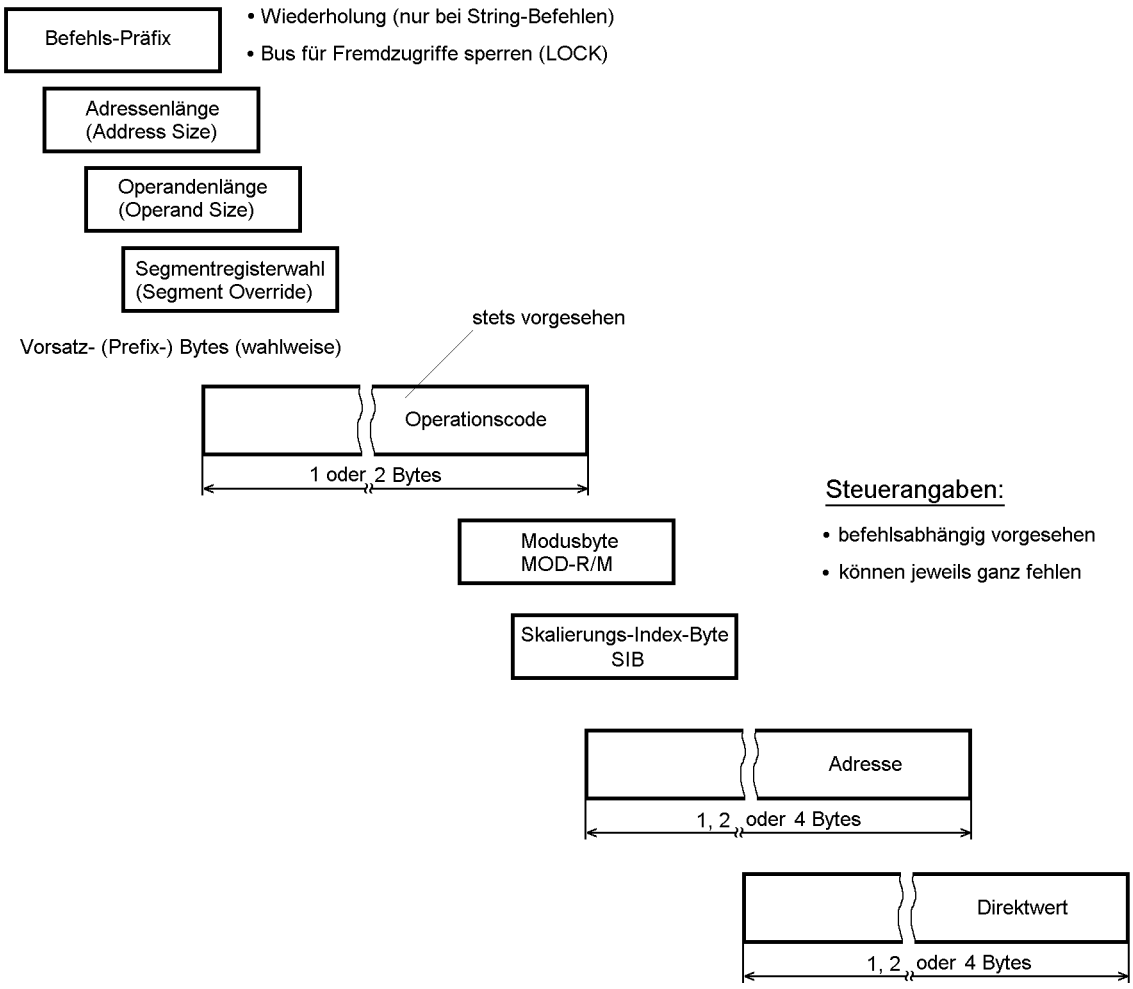


a) MMX, 3DNow

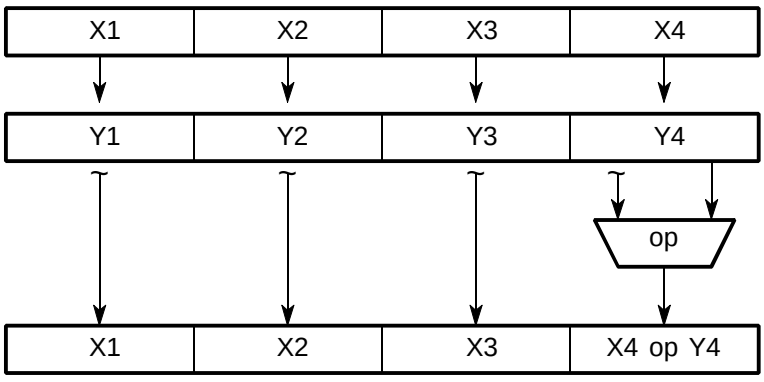


b) SSE

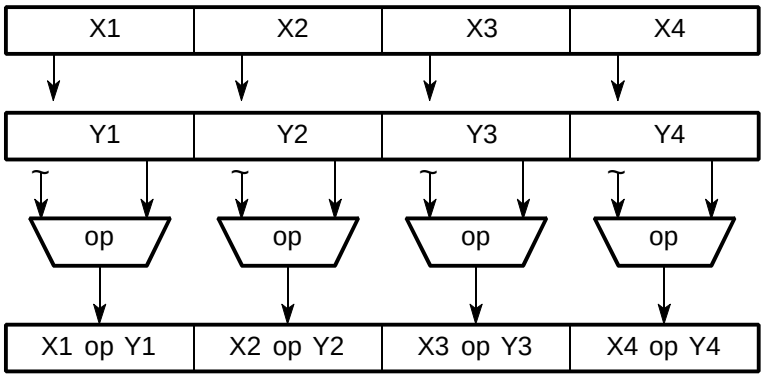


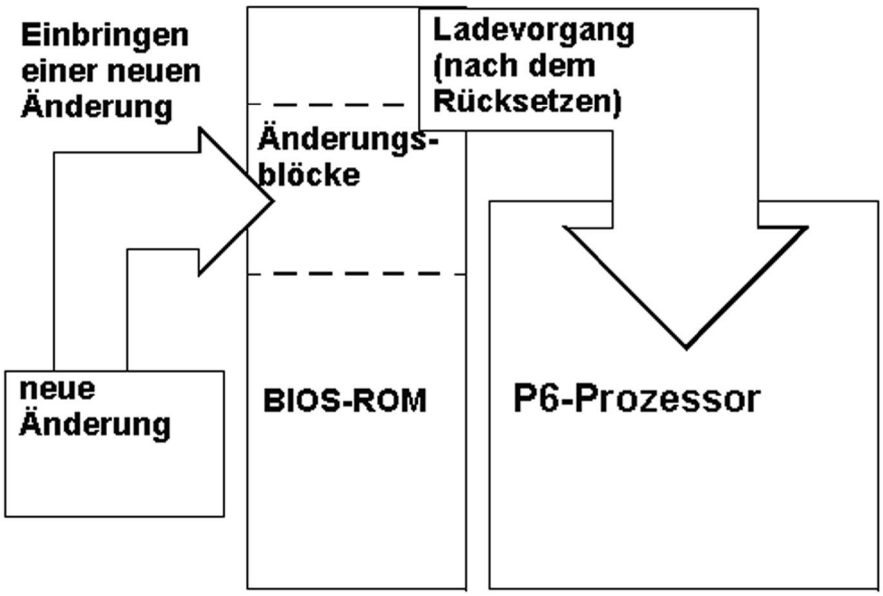

Befehls-Präfix
• Wiederholung (nur bei String-Befehlen)
• Bus für Fremdzugriffe sperren (LOCK)
Adressenlänge
(Address Size)
Operandenlänge
(Operand Size)
Segmentregisterwahl
(Segment Override)
Vorsatz- (Prefix-) Bytes (wahlweise)
stets vorgesehen
Operationscode
1 oder 2 Bytes
Modusbyte
MOD-R/M
Skalierungs-Index-Byte
SIB
Adresse
1, 2 oder 4 Bytes
Direktwert
1, 2 oder 4 Bytes
Steuerangaben:
• befehlsabhängig vorgesehen
• können jeweils ganz fehlen

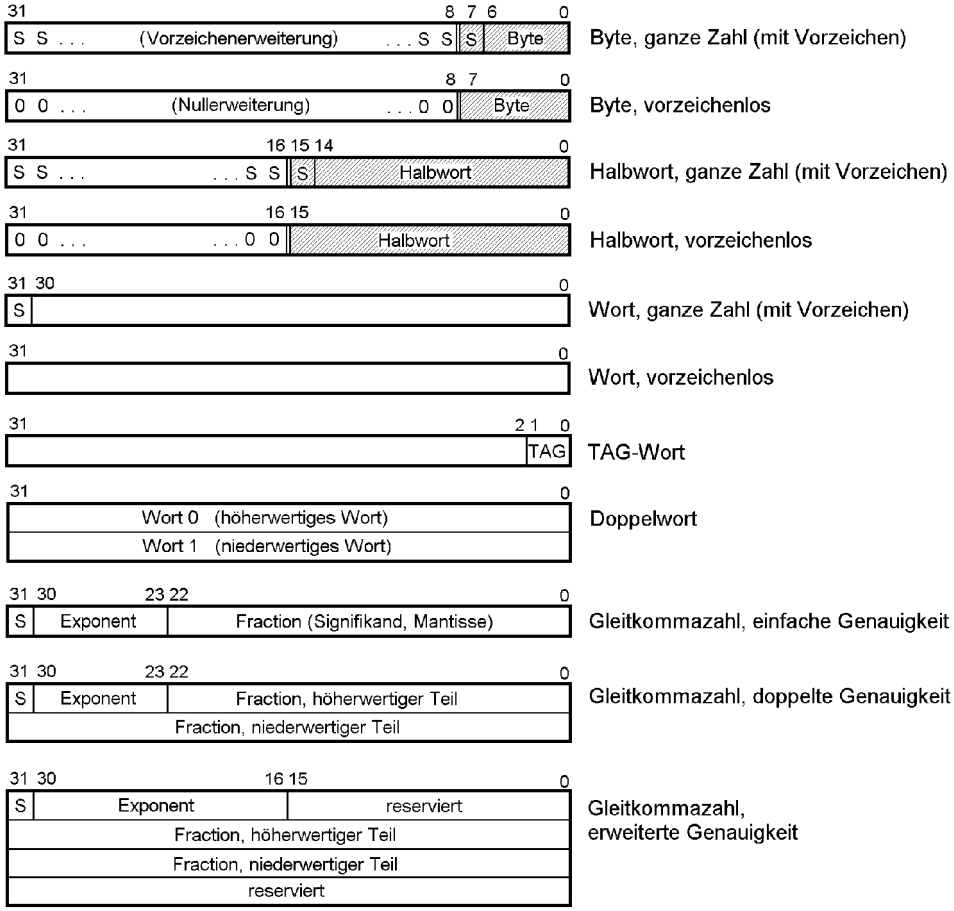
a)

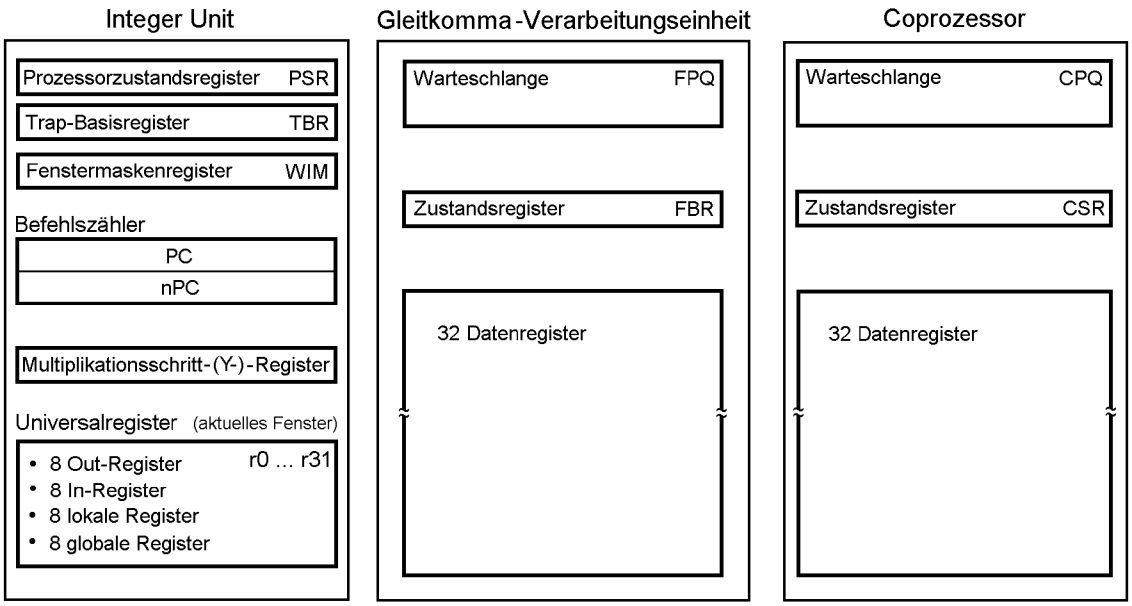

X1
X2
X3
X4
Y1
Y2
Y3
Y4
op
X1
X2
X3
X4 op Y4

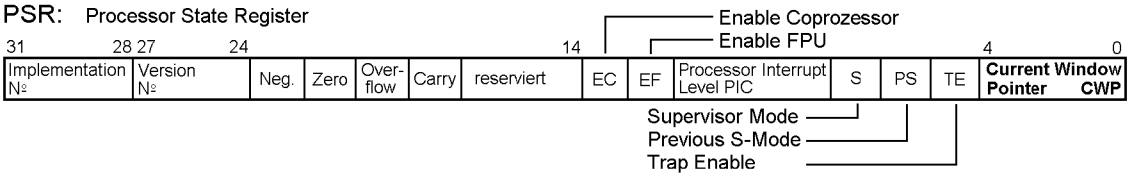
b)

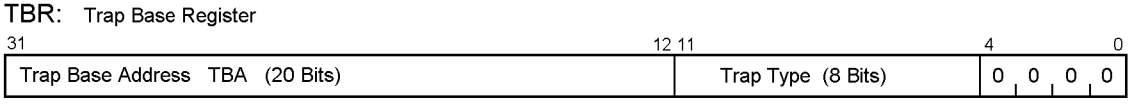

X1
X2
X3
X4
Y1
Y2
Y3
Y4
op
op
op
op
X1 op Y1
X2 op Y2
X3 op Y3
X4 op Y4

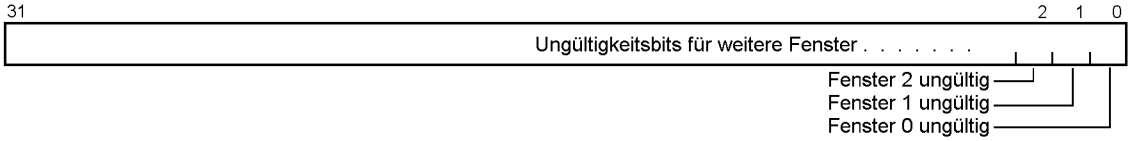

Einbringen einer neuen Änderung
Ladevorgang (nach dem Rücksetzen)
Änderungs-blöcke
neue Änderung
BIOS-ROM
P6-Prozessor

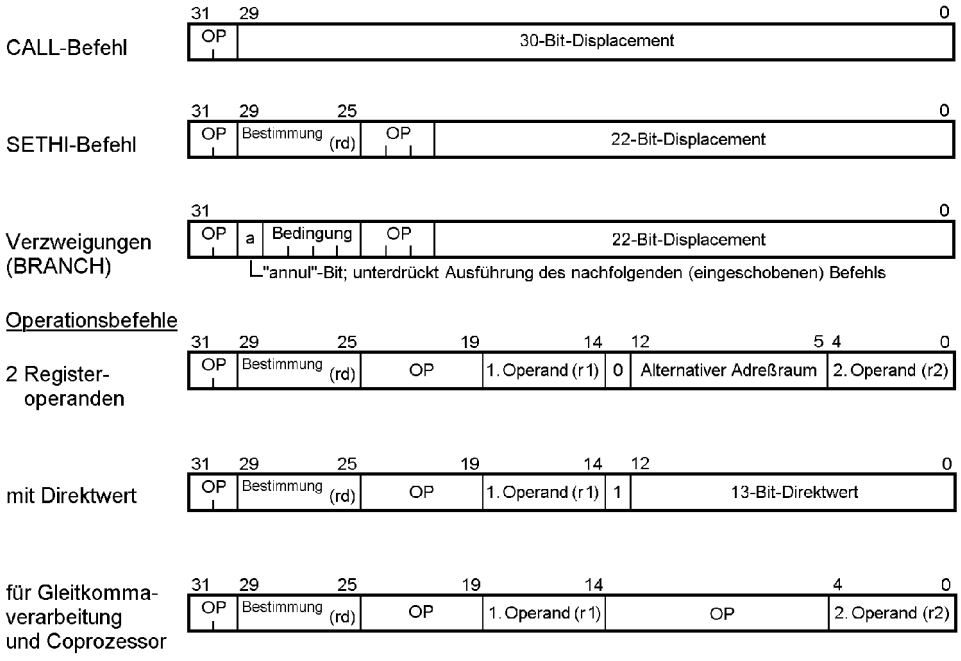

31 8 7 6 0
S S . . . (Vorzeichenerweiterung) . . . S S S Byte
Byte, ganze Zahl (mit Vorzeichen)
31 8 7 0
0 0 . . . (Nullerweiterung) . . . 0 0 Byte
Byte, vorzeichenlos
31 16 15 14 0
S S . . . . . . S S S Halbwort
Halbwort, ganze Zahl (mit Vorzeichen)
31 16 15 0
0 0 . . . . . . 0 0 Halbwort
Halbwort, vorzeichenlos
31 30 0
S
Wort, ganze Zahl (mit Vorzeichen)
31 0
Wort, vorzeichenlos
31 2 1 0
TAG
TAG-Wort
31 0
Wort 0 (höherwertiges Wort)
Wort 1 (niederwertiges Wort)
Doppelwort
31 30 23 22 0
S Exponent Fraction (Signifikand, Mantisse)
Gleitkommazahl, einfache Genauigkeit
31 30 23 22 0
S Exponent Fraction, höherwertiger Teil
Fraction, niederwertiger Teil
Gleitkommazahl, doppelte Genauigkeit
31 30 16 15 0
S Exponent reserviert
Fraction, höherwertiger Teil
Fraction, niederwertiger Teil
reserviert
Gleitkommazahl, erweiterte Genauigkeit

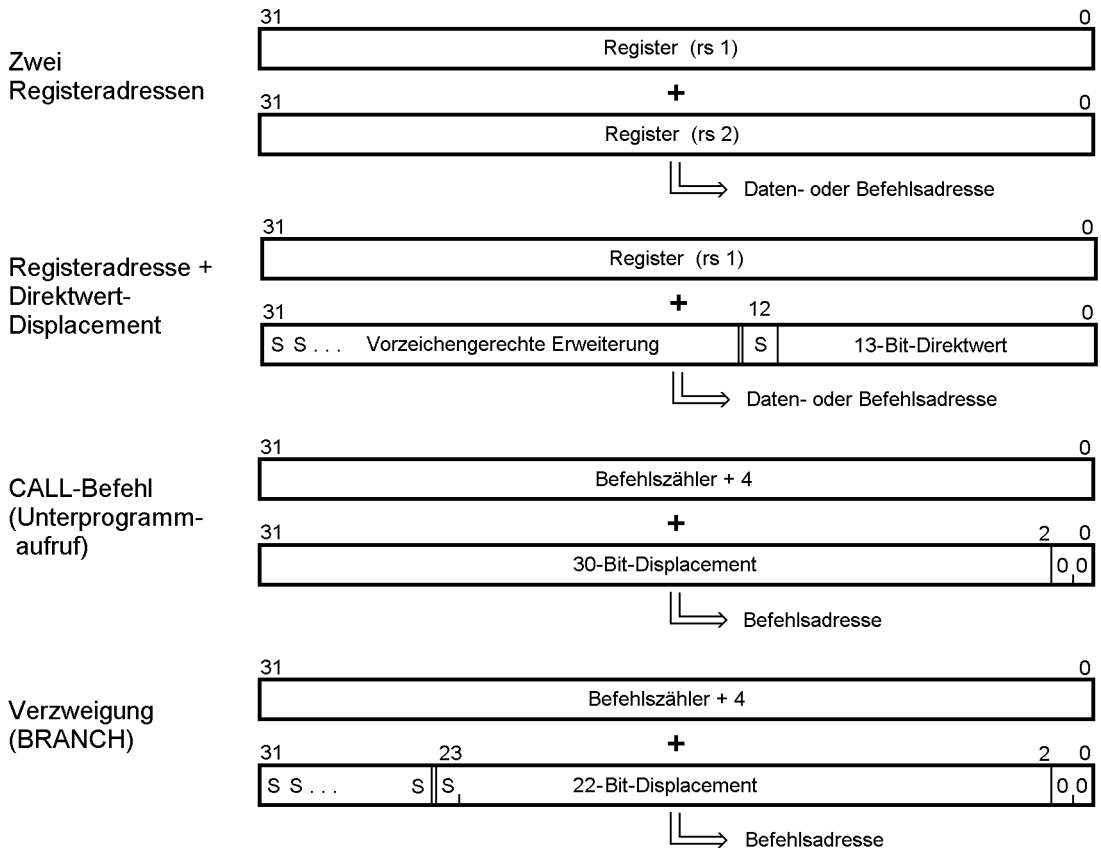

Integer Unit
Prozessorzustandsregister PSR
Trap-Basisregister TBR
Fenstermaskenregister WIM
Befehlszähler
PC
nPC
Multiplikationsschritt-(Y-)-Register
Universalregister (aktuelles Fenster)
• 8 Out-Register r0 ... r31
• 8 In-Register
• 8 lokale Register
• 8 globale Register
Gleitkomma-Verarbeitungseinheit
Warteschlange FPQ
Zustandsregister FBR
32 Datenregister
Coprozessor
Warteschlange CPQ
Zustandsregister CSR
32 Datenregister

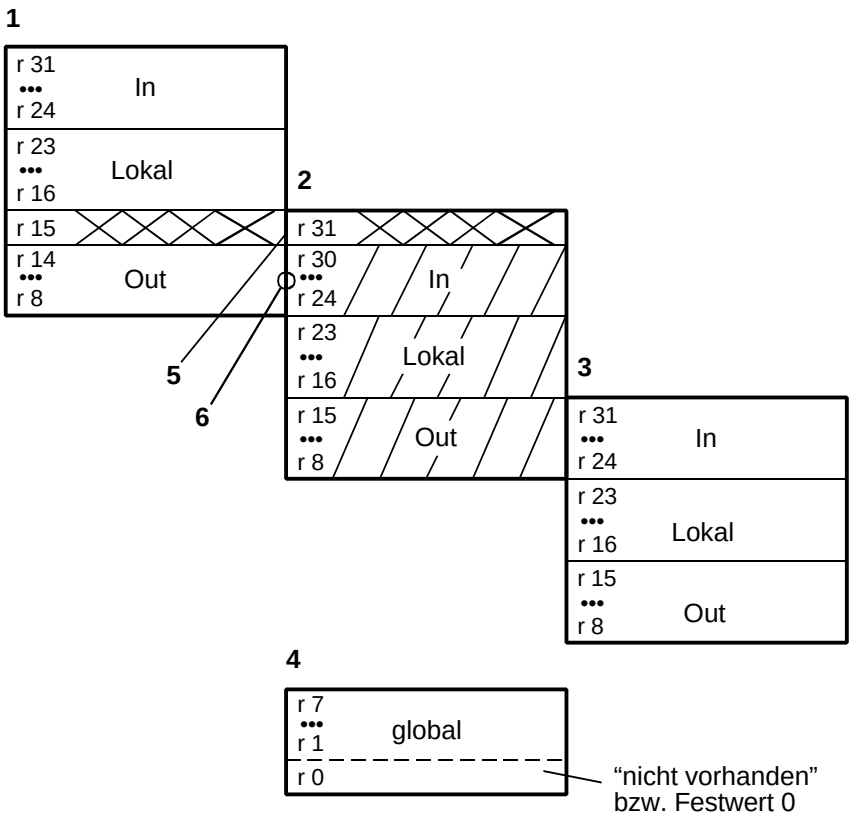

PSR: Processor State Register
Enable Coprozessor
Enable FPU
31 28 27 24 14 4 0
Implementation №
Version №
Neg.
Zero
Over-flow
Carry
reserviert
EC
EF
Processor Interrupt Level PIC
S
PS
TE
Current Window Pointer CWP
Supervisor Mode
Previous S-Mode
Trap Enable


TBR: Trap Base Register
31 12 11 4 0
Trap Base Address TBA (20 Bits)
Trap Type (8 Bits)
0 0 0 0

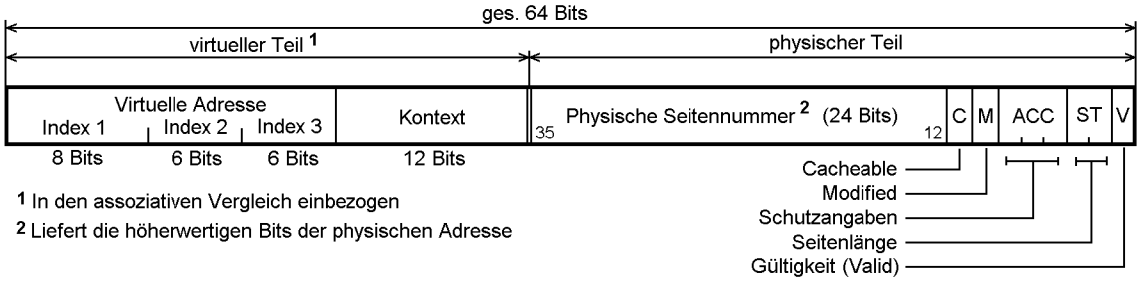

WIM: Window Invalid Mask
31 2 1 0
Ungültigkeitsbits für weitere Fenster . . . . . .
Fenster 2 ungültig
Fenster 1 ungültig
Fenster 0 ungültig


CALL-Befehl
31 29 0
OP
30-Bit-Displacement
SETHI-Befehl
31 29 25 0
OP
Bestimmung (rd)
OP
22-Bit-Displacement
Verzweigungen (BRANCH)
31 0
OP
a
Bedingung
OP
22-Bit-Displacement
"annul"-Bit; unterdrückt Ausführung des nachfolgenden (eingeschobenen) Befehls
Operationsbefehle
2 Register-operanden
31 29 25 19 14 12 5 4 0
OP
Bestimmung (rd)
OP
1. Operand (r1)
0
Alternativer Adreßraum
2. Operand (r2)
mit Direktwert
31 29 25 19 14 12 0
OP
Bestimmung (rd)
OP
1. Operand (r1)
1
13-Bit-Direktwert
für Gleitkomma-verarbeitung und Coprozessor
31 29 25 19 14 4 0
OP
Bestimmung (rd)
OP
1. Operand (r1)
OP
2. Operand (r2)


Zwei Registeradressen
31
0
Register (rs 1)
+
31
0
Register (rs 2)
Daten- oder Befehlsadresse
Registeradresse + Direktwert-Displacement
31
0
Register (rs 1)
+
31
12
0
S S . . . Vorzeichengerechte Erweiterung
S
13-Bit-Direktwert
Daten- oder Befehlsadresse
CALL-Befehl (Unterprogramm-aufruf)
31
0
Befehlszähler + 4
+
31
2
0
30-Bit-Displacement
0 0
Befehlsadresse
Verzweigung (BRANCH)
31
0
Befehlszähler + 4
+
31
23
2
0
S S . . . S
S
22-Bit-Displacement
0 0
Befehlsadresse


1
r 31 ••• r 24
In
r 23 ••• r 16
Lokal
r 15
r 14 ••• r 8
Out
2
r 31
r 30 ••• r 24
In
r 23 ••• r 16
Lokal
r 15 ••• r 8
Out
3
r 31 ••• r 24
In
r 23 ••• r 16
Lokal
r 15 ••• r 8
Out
4
r 7 ••• r 1
global
r 0
“nicht vorhanden” bzw. Festwert 0
5
6

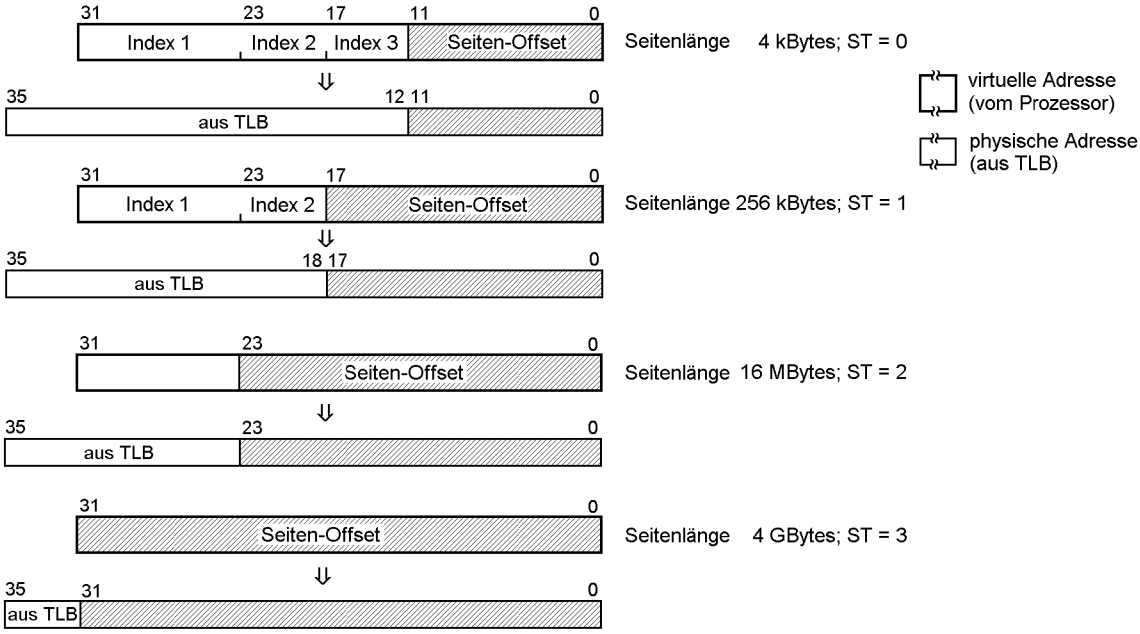
TLB-Eintrag:

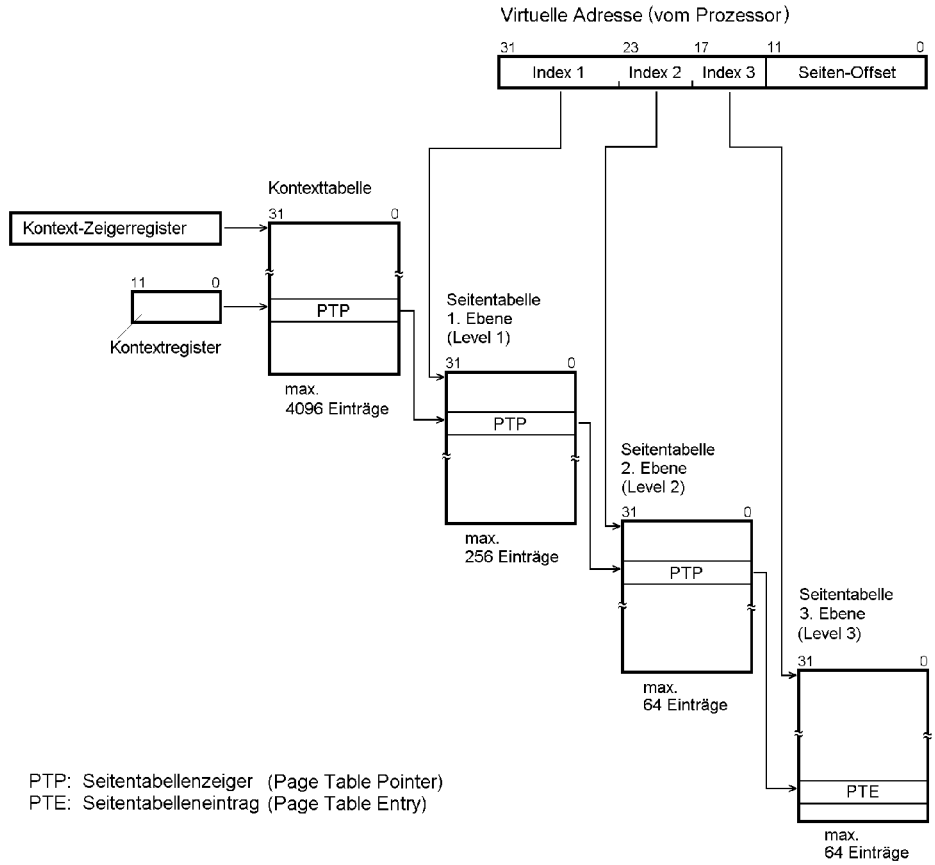


1 In den assoziativen Vergleich einbezogen

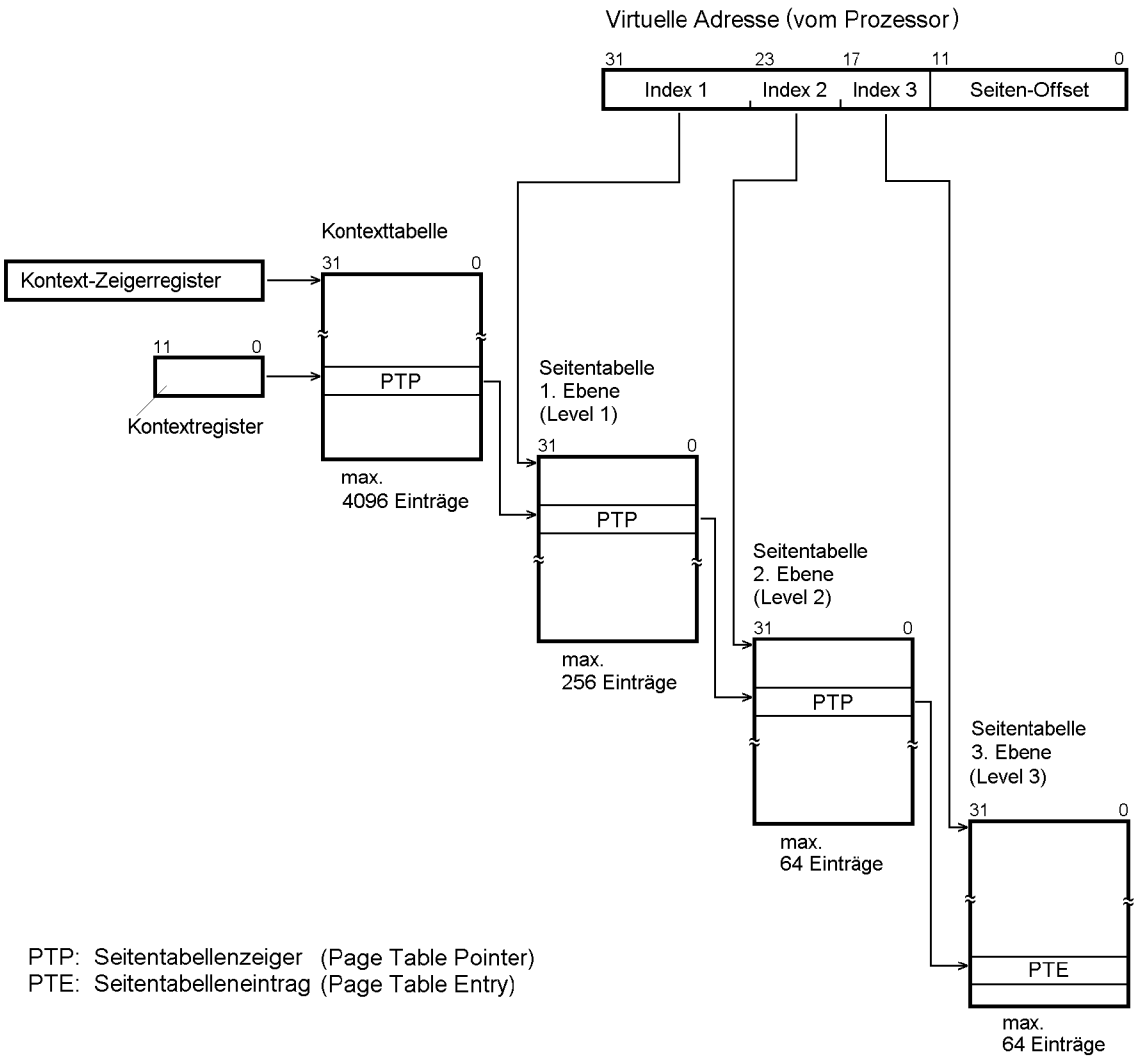
2 Liefert die höherwertigen Bits der physischen Adresse

Adreßumsetzung:

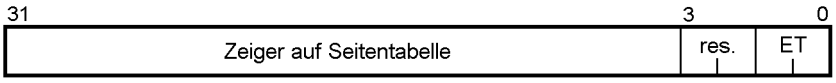




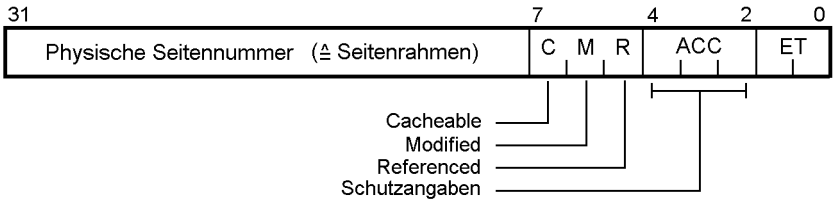
PTP: Seitentabellenzeiger (Page Table Pointer)
PTE: Seitentabelleneintrag (Page Table Entry)



Seitentabellenzeiger (Page Table Pointer) PTP

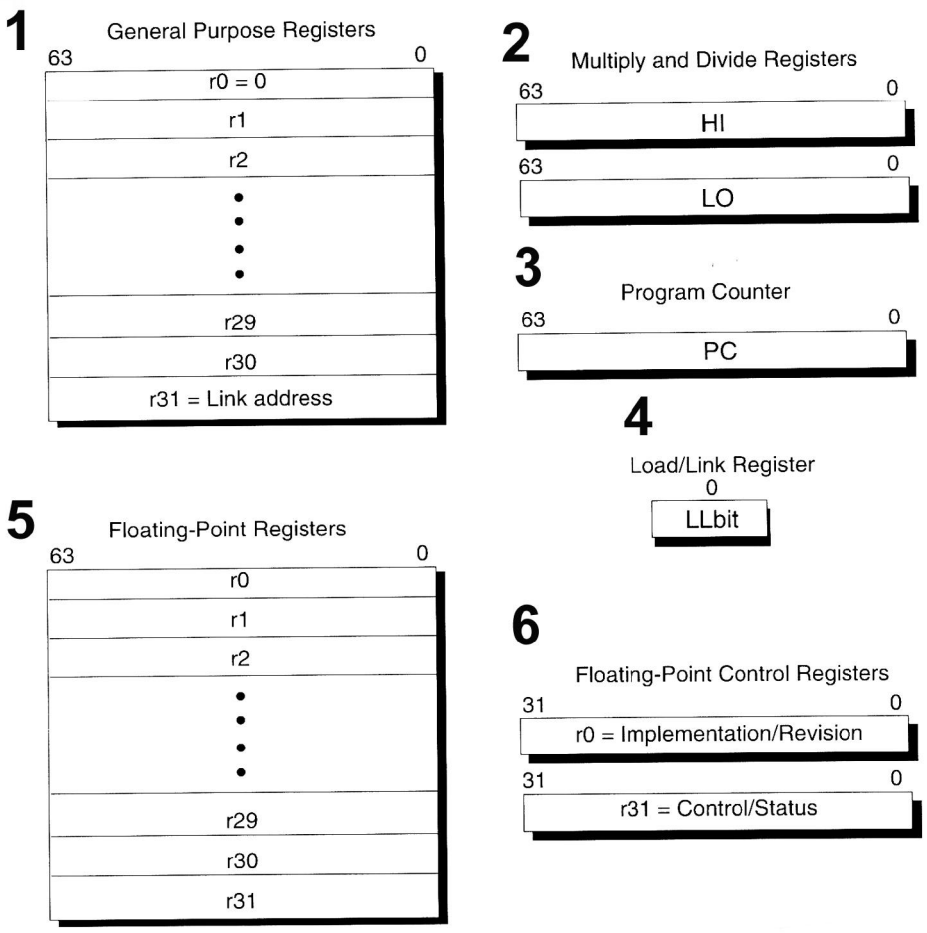


Seitentabelleneintrag (Page Table Entry) PTE

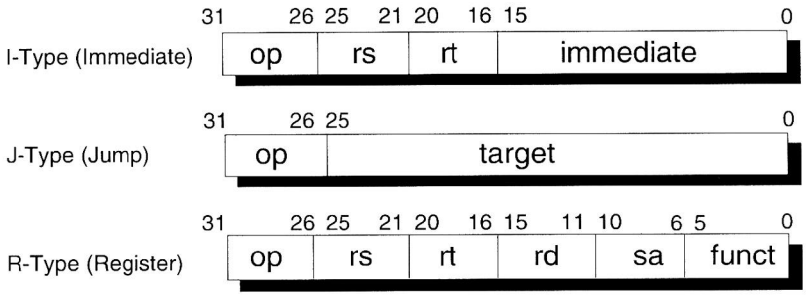


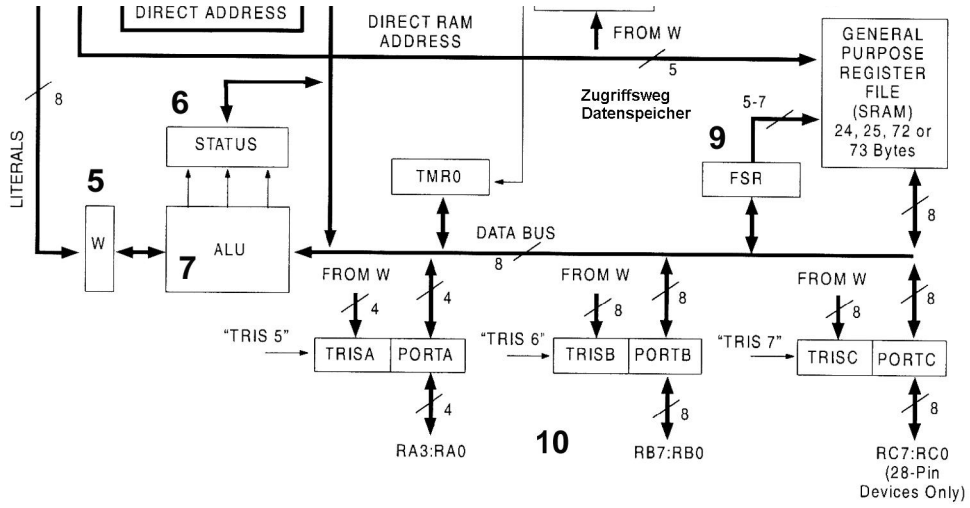
Formatkennung ET (Entry Type):

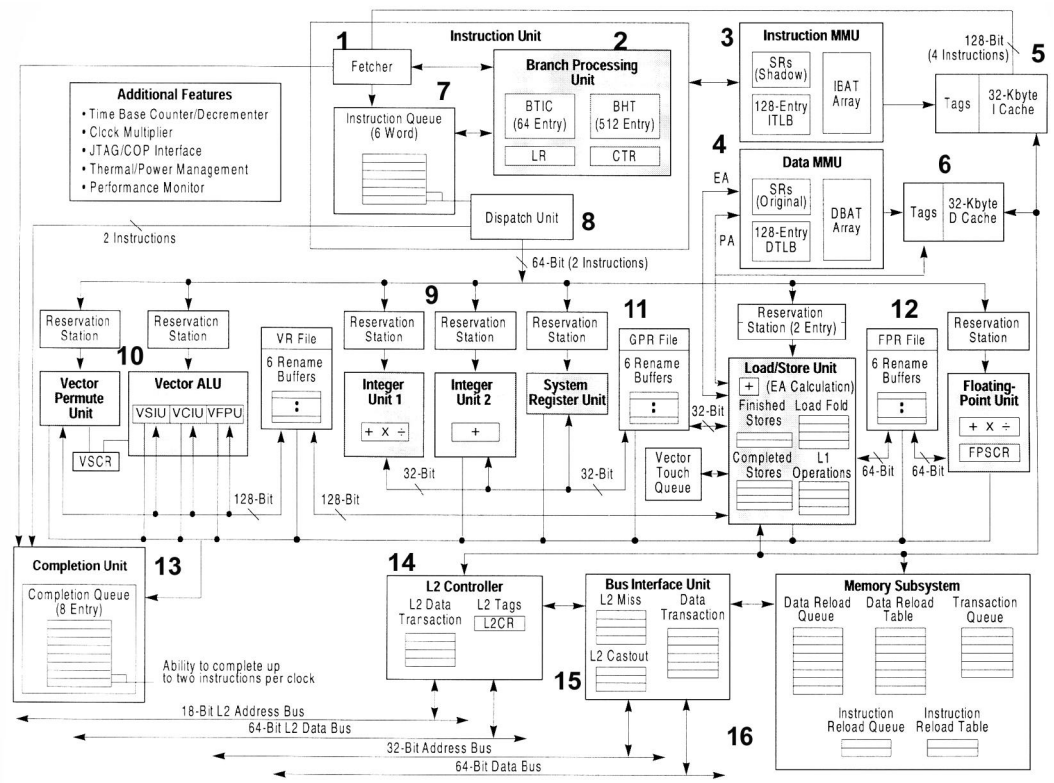
- 0 : ungültig
- 1 : Seitentabellenzeiger
- 2 : Seitentabelleneintrag
- 3 : reserviert

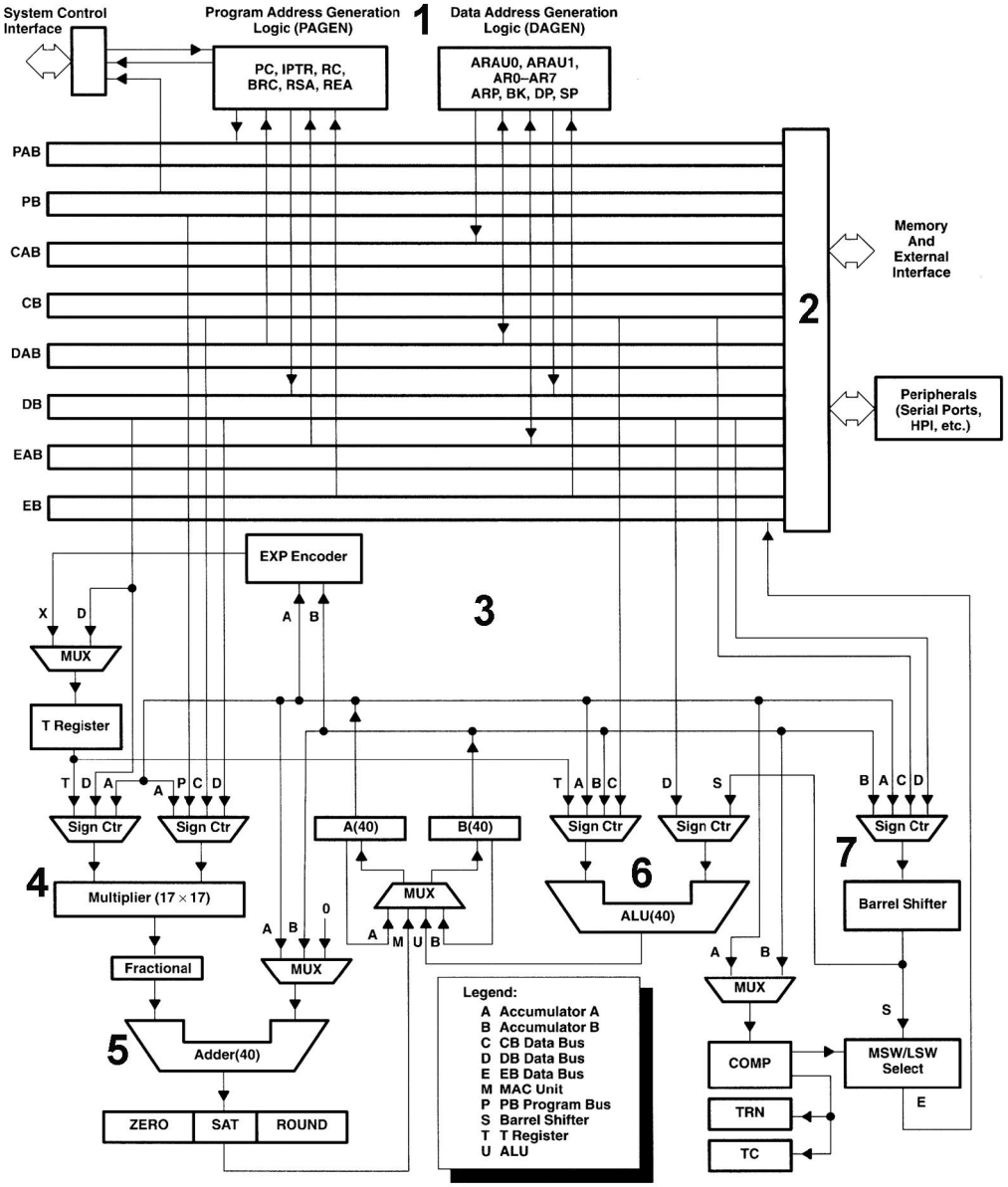


Befehlsformate:






Additional Features
• Time Base Counter/Decrementer
• Clock Multiplier
• JTAG/COP Interface
• Thermal/Power Management
• Performance Monitor
1
Instruction Unit
2
Fetcher
Branch Processing Unit
BTIC (64 Entry)
BHT (512 Entry)
LR
CTR
7
Instruction Queue (6 Word)
Dispatch Unit
8
2 Instructions
64-Bit (2 Instructions)
3
Instruction MMU
SRs (Shadow)
128-Entry ITLB
IBAT Array
128-Bit (4 Instructions)
5
Tags
32-Kbyte I Cache
4
Data MMU
SRs (Original)
128-Entry DTLB
DBAT Array
EA
PA
6
Tags
32-Kbyte D Cache
9
Reservation Station
Reservation Station
Reservation Station
Reservation Station
Reservation Station
10
Vector Permute Unit
Vector ALU
VSIU
VCIU
VFPU
VSCR
VR File
6 Rename Buffers
Integer Unit 1
+ X ÷
Integer Unit 2
+
System Register Unit
11
GPR File
6 Rename Buffers
Reservation Station (2 Entry)
Load/Store Unit
+
(EA Calculation)
Finished Stores
Load Fold
Completed Stores
L1 Operations
Vector Touch Queue
12
FPR File
6 Rename Buffers
Reservation Station
Floating-Point Unit
+ X ÷
FPSCR
32-Bit
32-Bit
32-Bit
64-Bit
64-Bit
128-Bit
128-Bit
Completion Unit
13
Completion Queue (8 Entry)
Ability to complete up to two instructions per clock
14
L2 Controller
L2 Data Transaction
L2 Tags
L2CR
Bus Interface Unit
L2 Miss
Data Transaction
L2 Castout
15
Memory Subsystem
Data Reload Queue
Data Reload Table
Transaction Queue
Instruction Reload Queue
Instruction Reload Table
16
18-Bit L2 Address Bus
64-Bit L2 Data Bus
32-Bit Address Bus
64-Bit Data Bus



UPMC3 SPR 941
UPMC4 SPR 942

Sampled Instruction Address

USIAR SPR 939

Monitor Control

UMMCR0 SPR 936
UMMCR1 SPR 940
UMMCR2 SPR 928

Breakpoint Address Mask Register

UBAMR SPR 935

FPR31

5

Condition Register

CR

Floating-Point Status and Control Register 3

FPSCR

AltiVec Registers

AltiVec Save Register

VRSAVE SPR 256

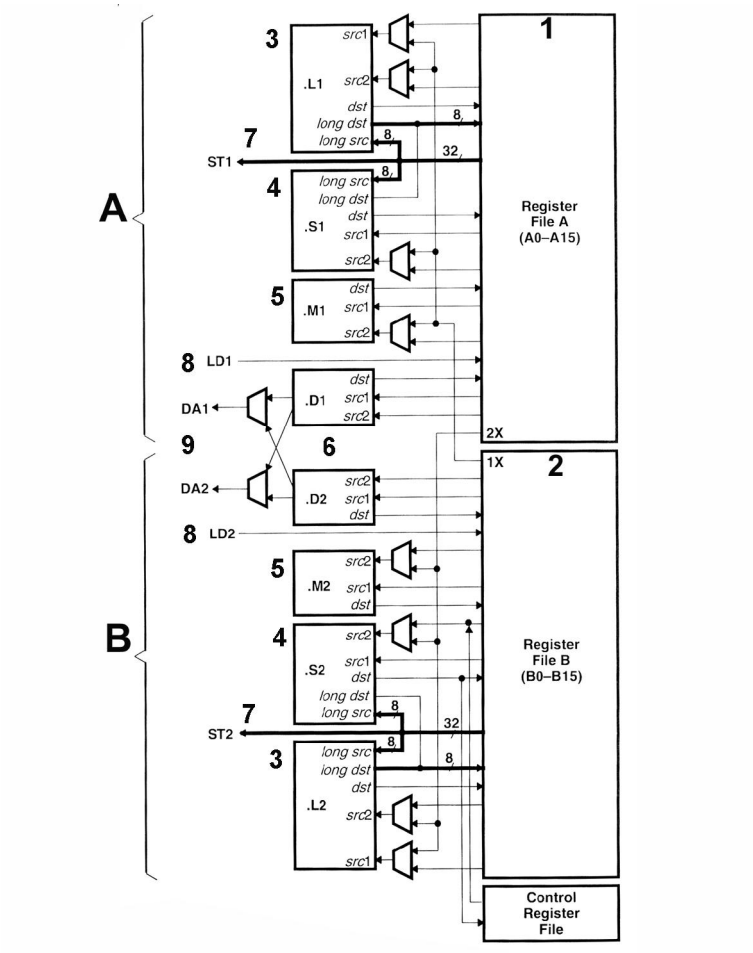
Vector Status and Control Register

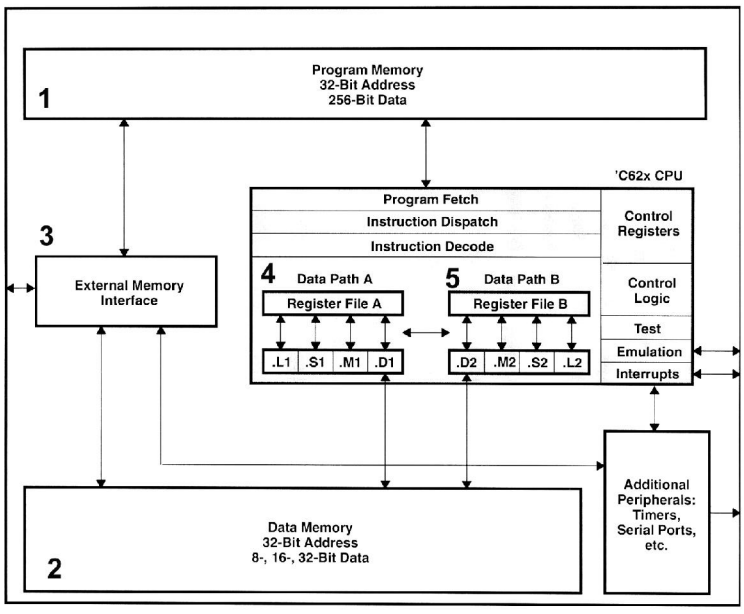
VSCR

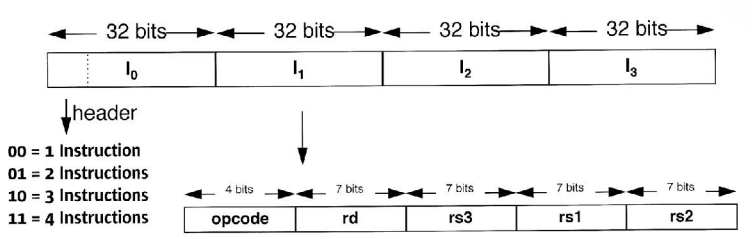
4

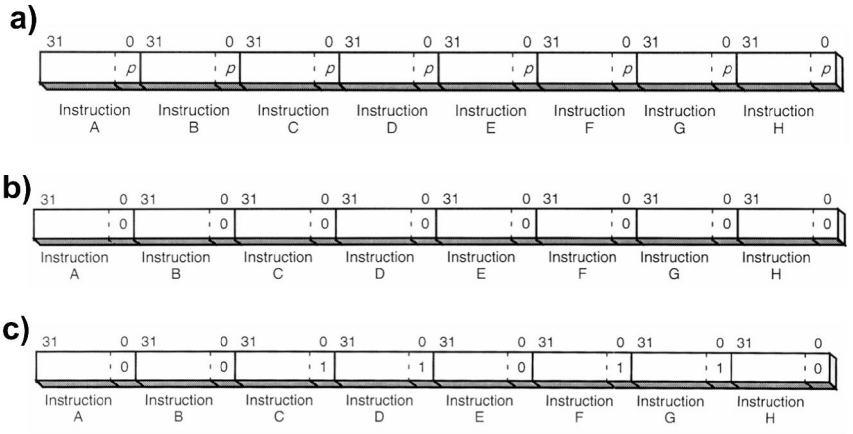
Vector Registers

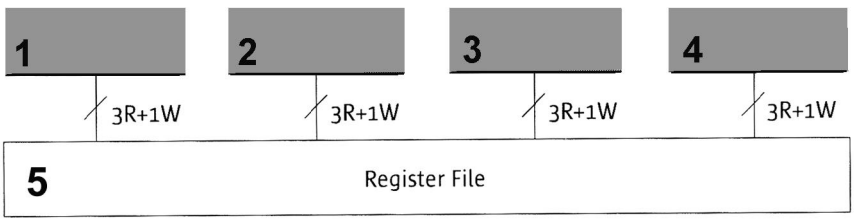
VR0
VR1
VR31

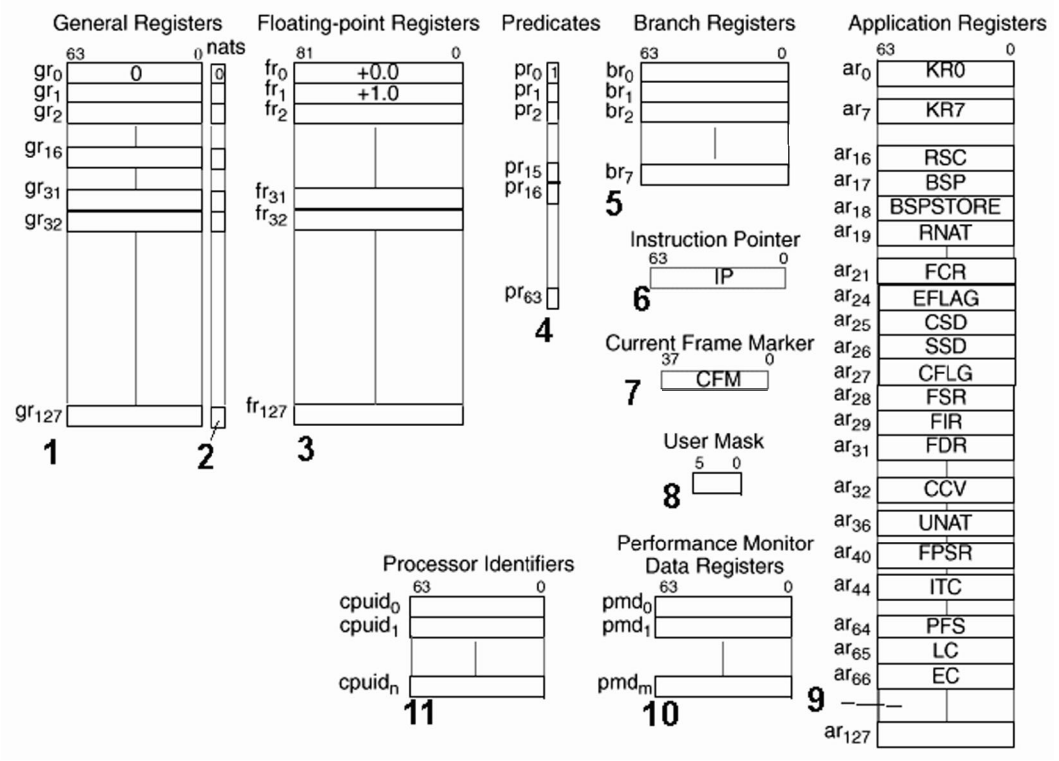

A
B
1
2
3
4
5
6
7
8
9
.L1
.S1
.M1
.D1
.D2
.M2
.S2
.L2
src1
src2
dst
long dst
long src
ST1
ST2
LD1
LD2
DA1
DA2
8
32
2X
1X
Register File A (A0–A15)
Register File B (B0–B15)
Control Register File

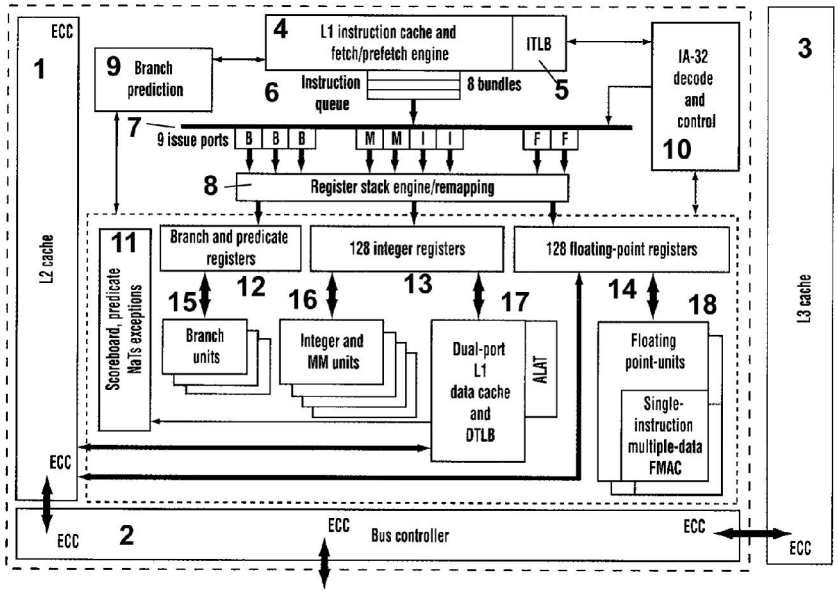

1
Program Memory
32-Bit Address
256-Bit Data
'C62x CPU
Program Fetch
Instruction Dispatch
Instruction Decode
Control Registers
3
External Memory Interface
4
Data Path A
Register File A
5
Data Path B
Register File B
.L1
.S1
.M1
.D1
.D2
.M2
.S2
.L2
Control Logic
Test
Emulation
Interrupts
Additional Peripherals: Timers, Serial Ports, etc.
2
Data Memory
32-Bit Address
8-, 16-, 32-Bit Data


32 bits
32 bits
32 bits
32 bits
I_0
I_1
I_2
I_3
header
00 = 1 Instruction
01 = 2 Instructions
10 = 3 Instructions
11 = 4 Instructions
4 bits
7 bits
7 bits
7 bits
7 bits
opcode
rd
rs3
rs1
rs2


a)
b)
c)
31 0
p
0
1
Instruction A
Instruction B
Instruction C
Instruction D
Instruction E
Instruction F
Instruction G
Instruction H


1
2
3
4
3R+1W
3R+1W
3R+1W
3R+1W
5
Register File


General Registers
Floating-point Registers
Predicates
Branch Registers
Application Registers
nats
Instruction Pointer
IP
Current Frame Marker
CFM
User Mask
Processor Identifiers
Performance Monitor Data Registers
KR0
KR7
RSC
BSP
BSPSTORE
RNAT
FCR
EFLAG
CSD
SSD
CFLG
FSR
FIR
FDR
CCV
UNAT
FPSR
ITC
PFS
LC
EC


ECC
L1 instruction cache and fetch/prefetch engine
ITLB
Branch prediction
Instruction queue
8 bundles
IA-32 decode and control
9 issue ports
Register stack engine/remapping
Branch and predicate registers
128 integer registers
128 floating-point registers
Scoreboard, predicate NaTs exceptions
Branch units
Integer and MM units
Dual-port L1 data cache and DTLB
ALAT
Floating point-units
Single-instruction multiple-data FMAC
L2 cache
L3 cache
Bus controller