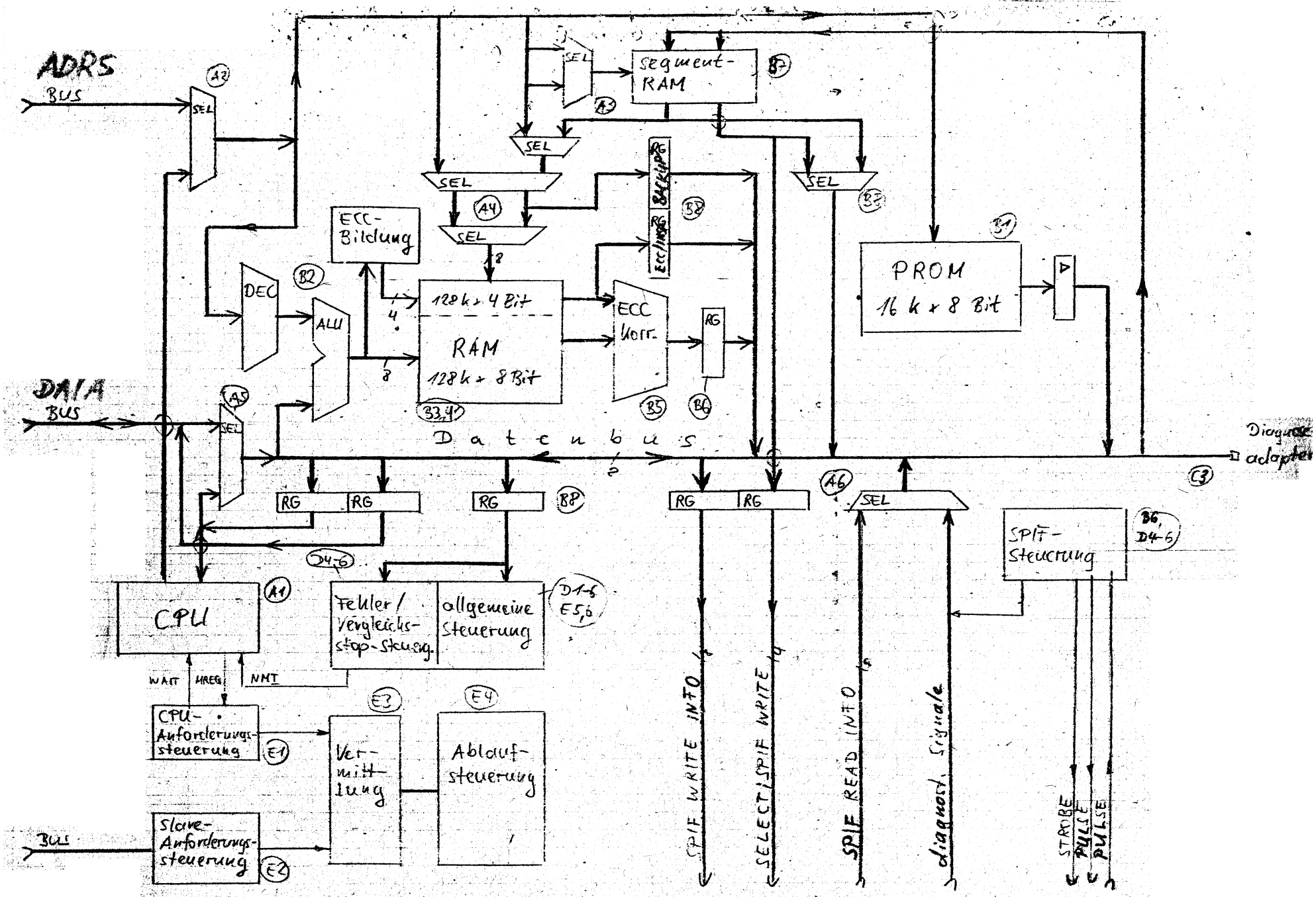
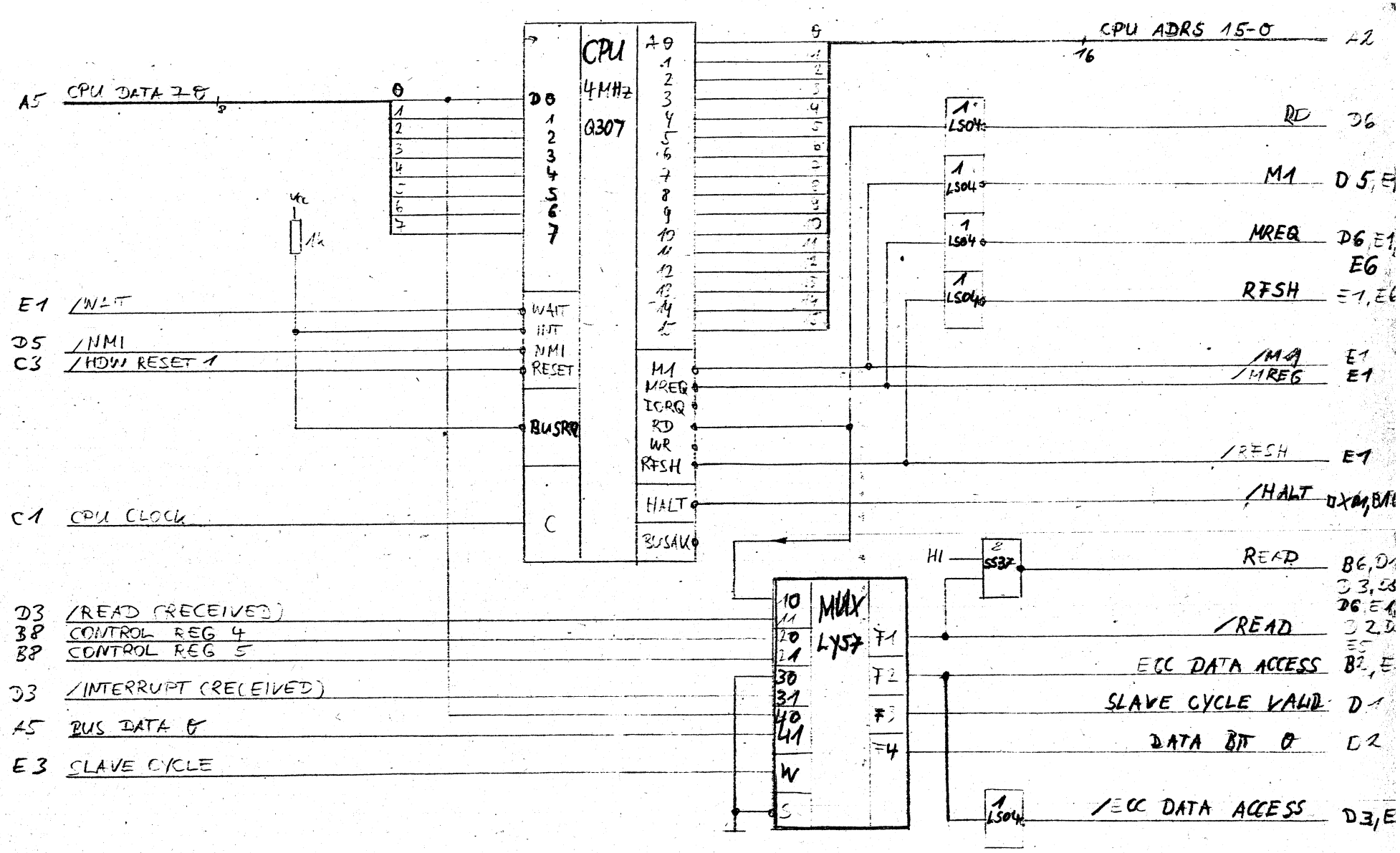


Special interface adapter

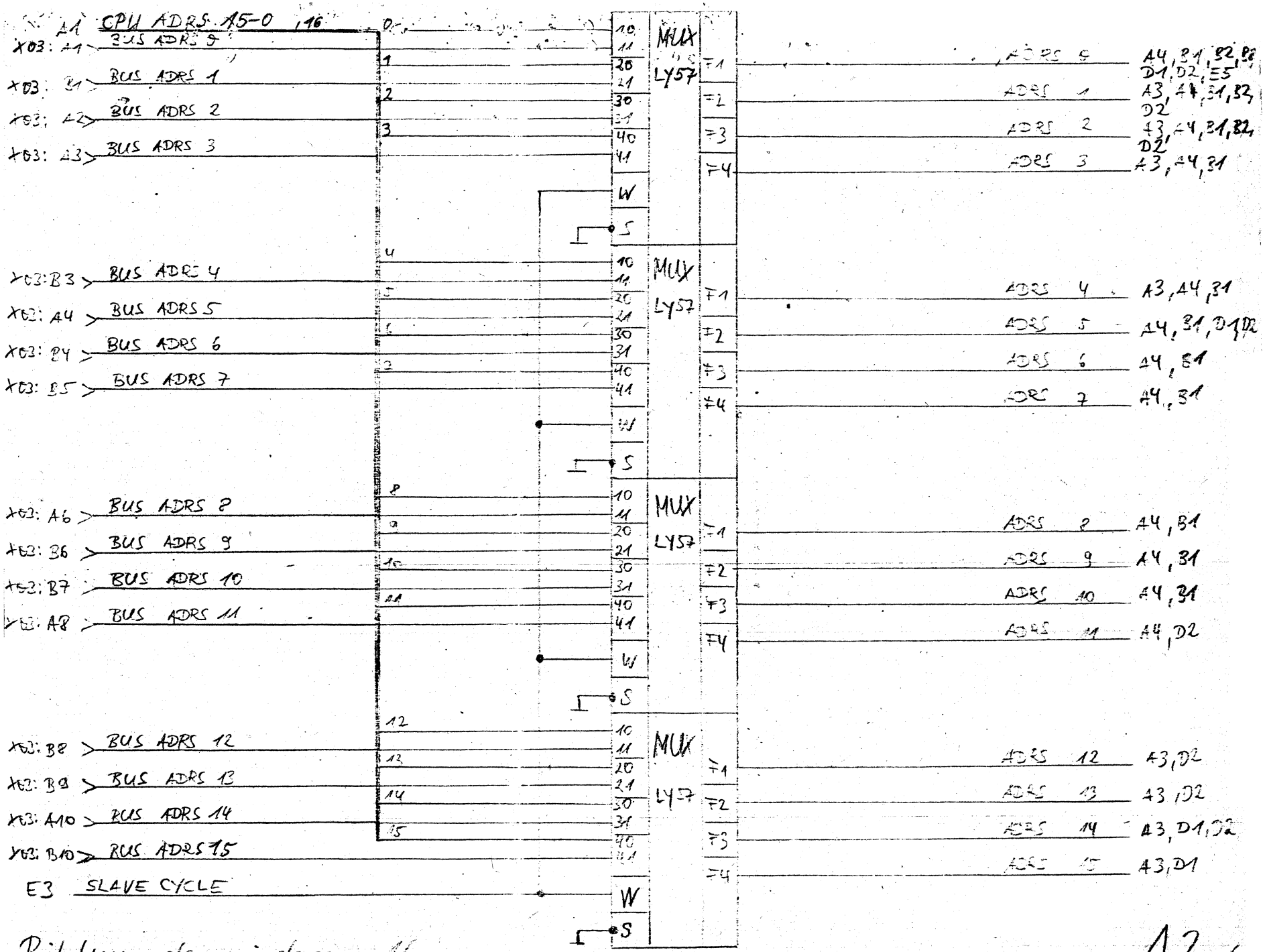
10.9.86 –
018 – 1152



SPIFAD

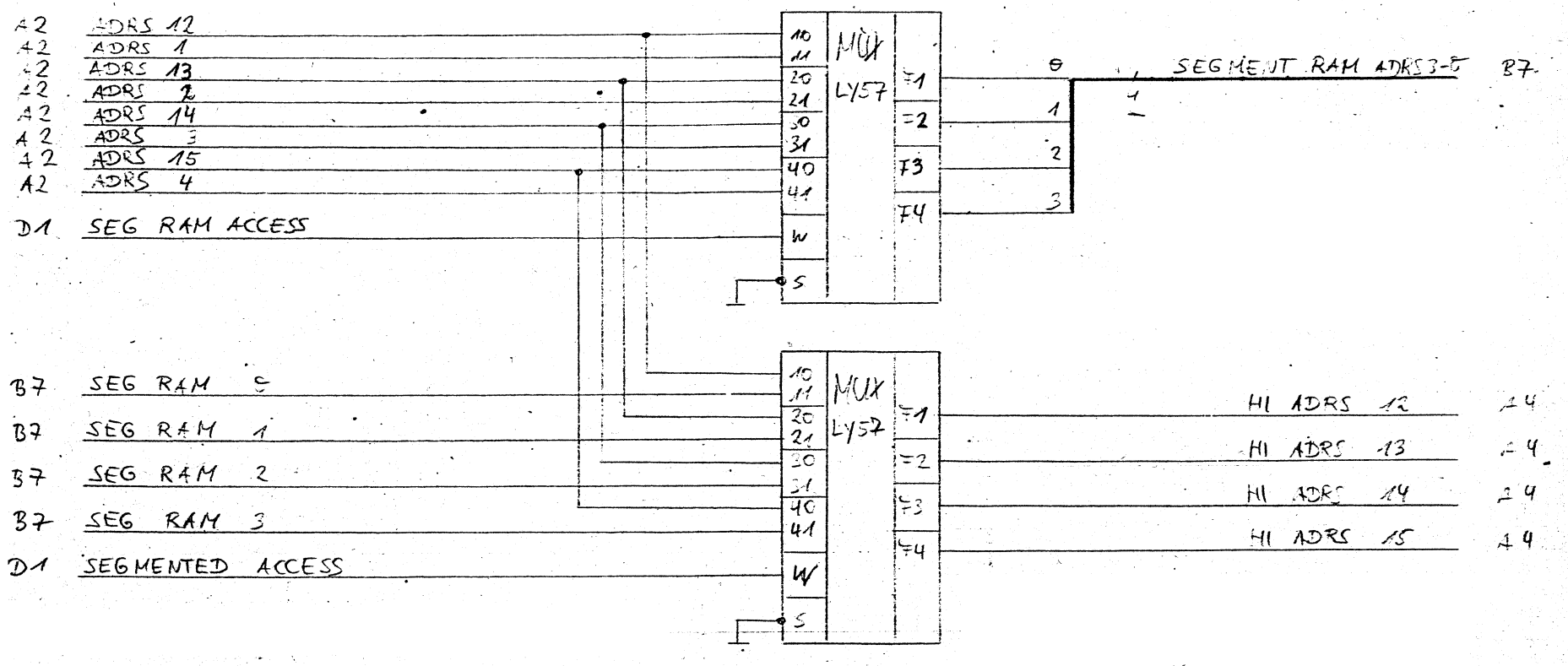
818-1152

A1



Bildung der niederen 16 Adressbits

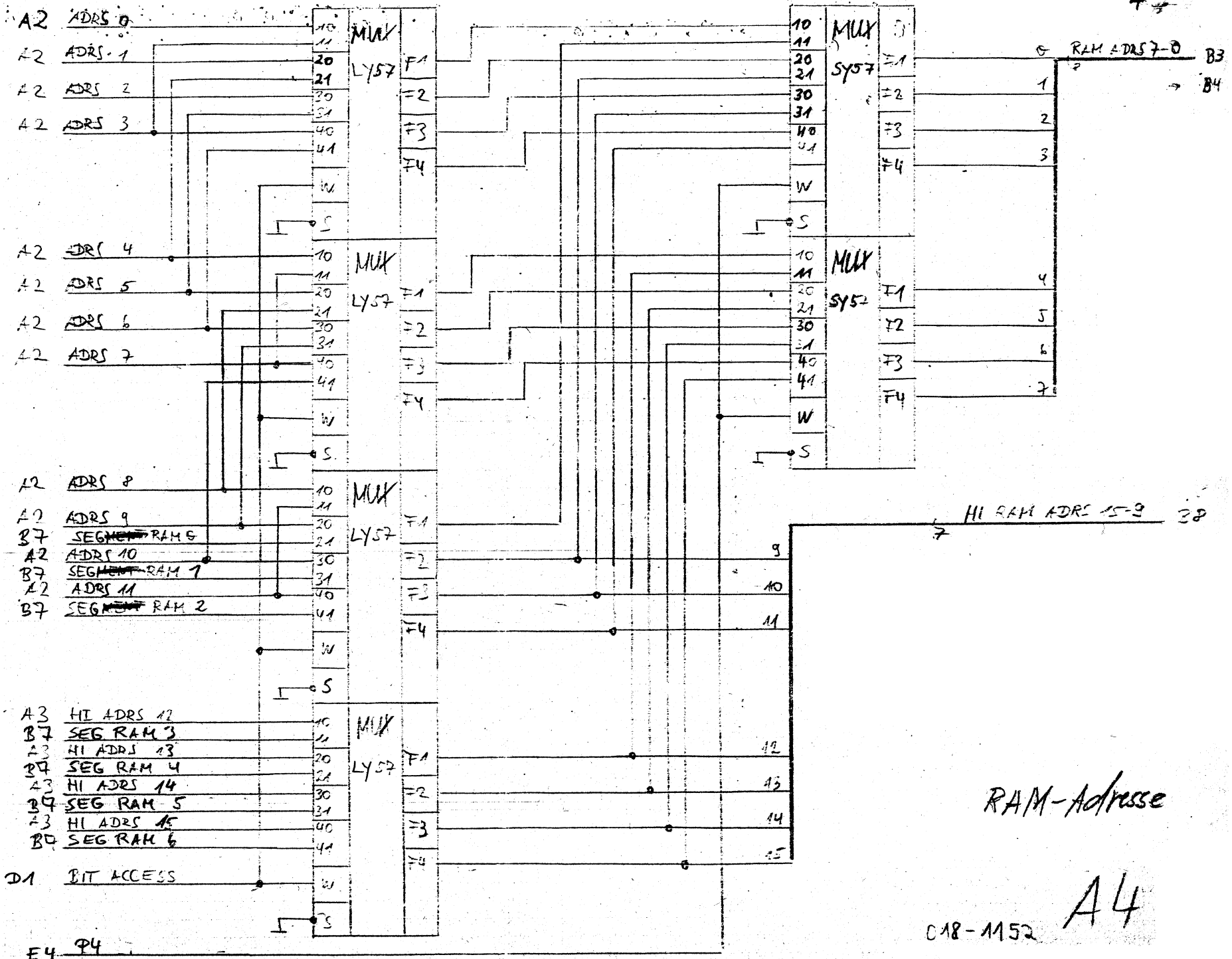
018-1152 A2

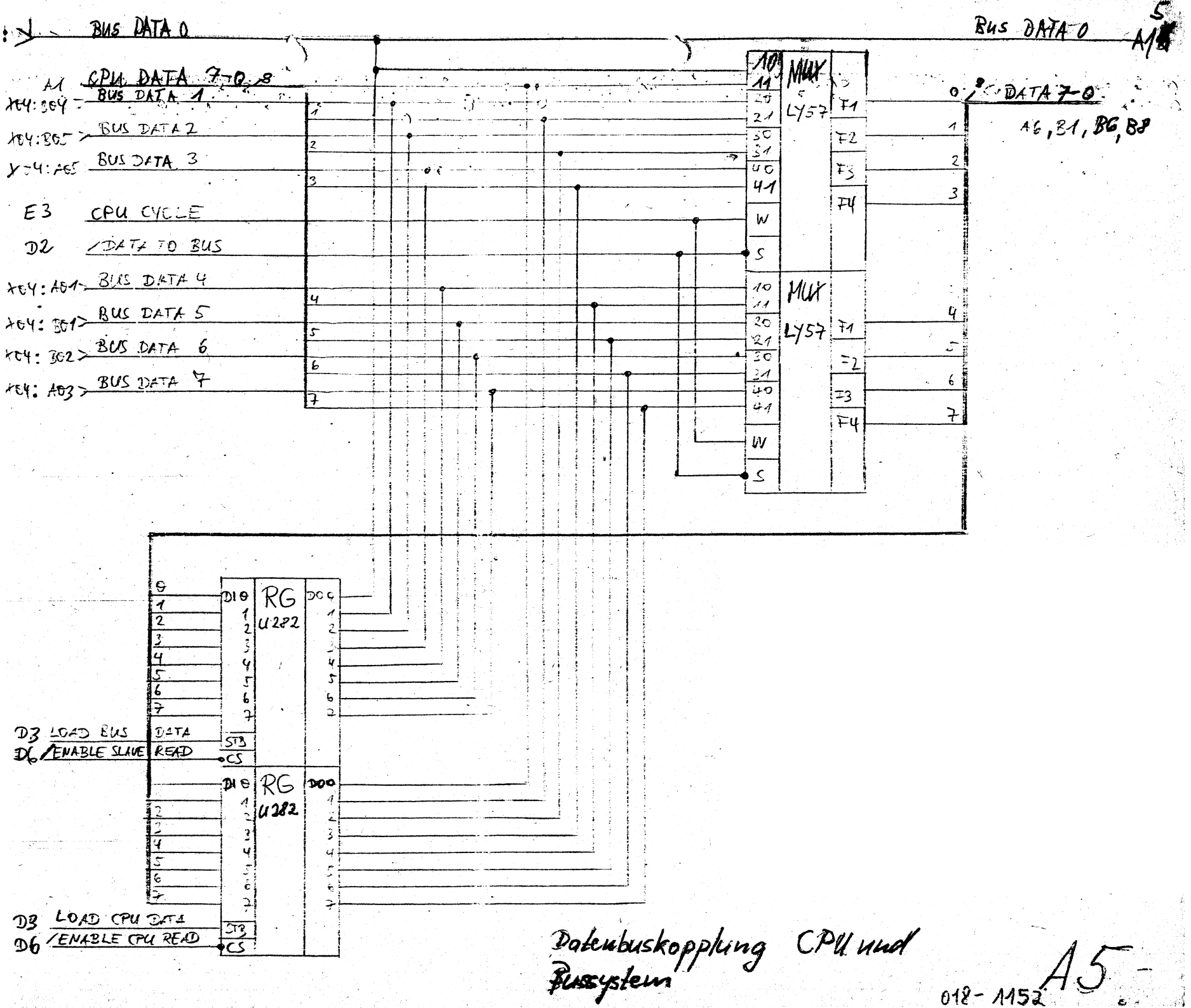


Adressierung Segment-RAM,
Adressenvorauswahl Bits -15-12

A3

018-1152

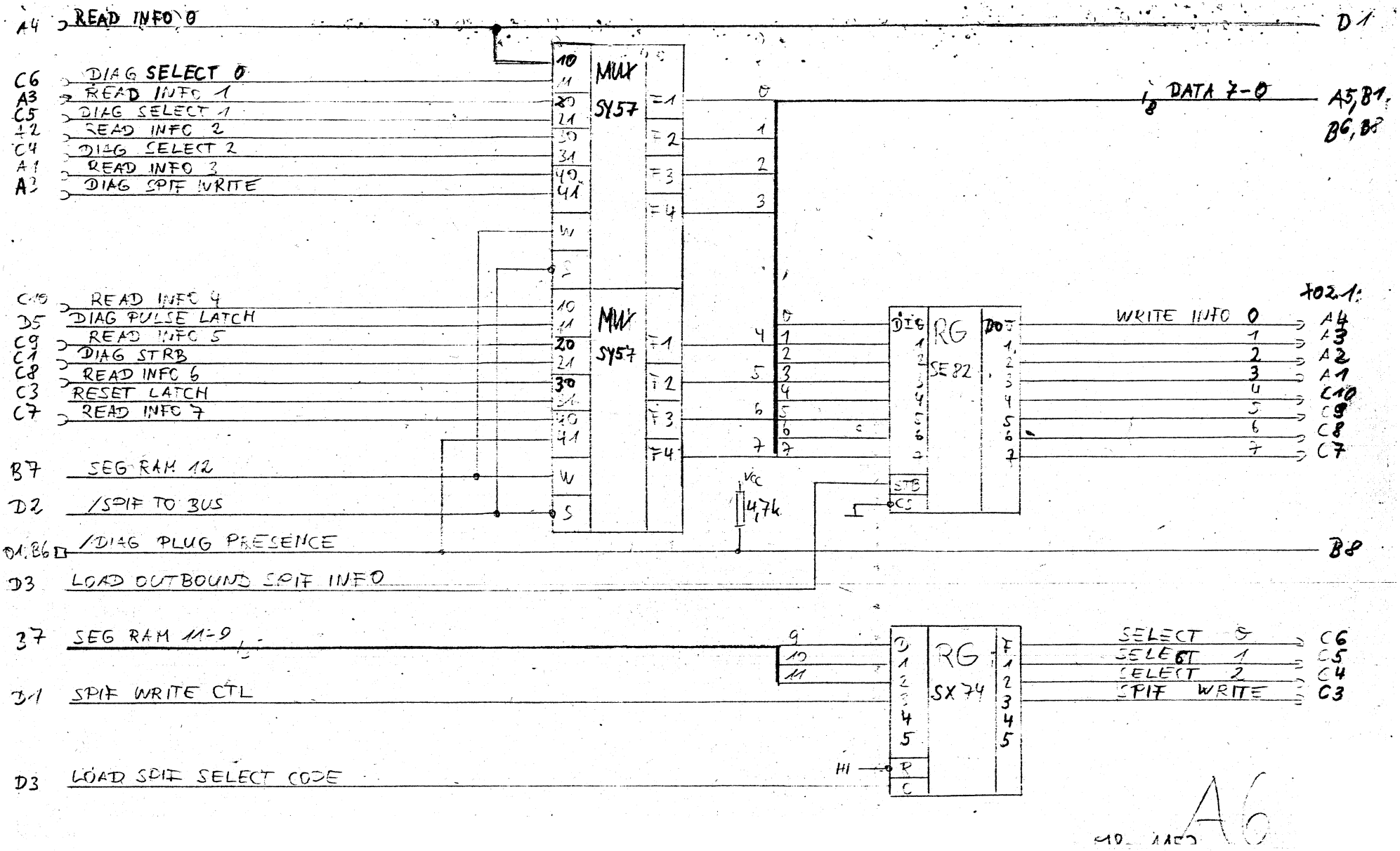

A2 ADRS 0
A2 ADRS 1
A2 ADRS 2
A2 ADRS 3
A2 ADRS 4
A2 ADRS 5
A2 ADRS 6
A2 ADRS 7
A2 ADRS 8
A2 ADRS 9
B7 SEG RAM 6
A2 ADRS 10
B7 SEG RAM 7
A2 ADRS 11
B7 SEG RAM 2
A3 HI ADRS 12
B7 SEG RAM 3
A3 HI ADRS 13
B7 SEG RAM 4
A3 HI ADRS 14
B7 SEG RAM 5
A3 HI ADRS 15
B7 SEG RAM 6
D1 BIT ACCESS
E4 P4
MUX LY57
MUX SY57
MUX SY52
RAM ADRS 7-0
B3
B4
HI RAM ADRS 15-9
B8
RAM-Adresse
A4
018-1152



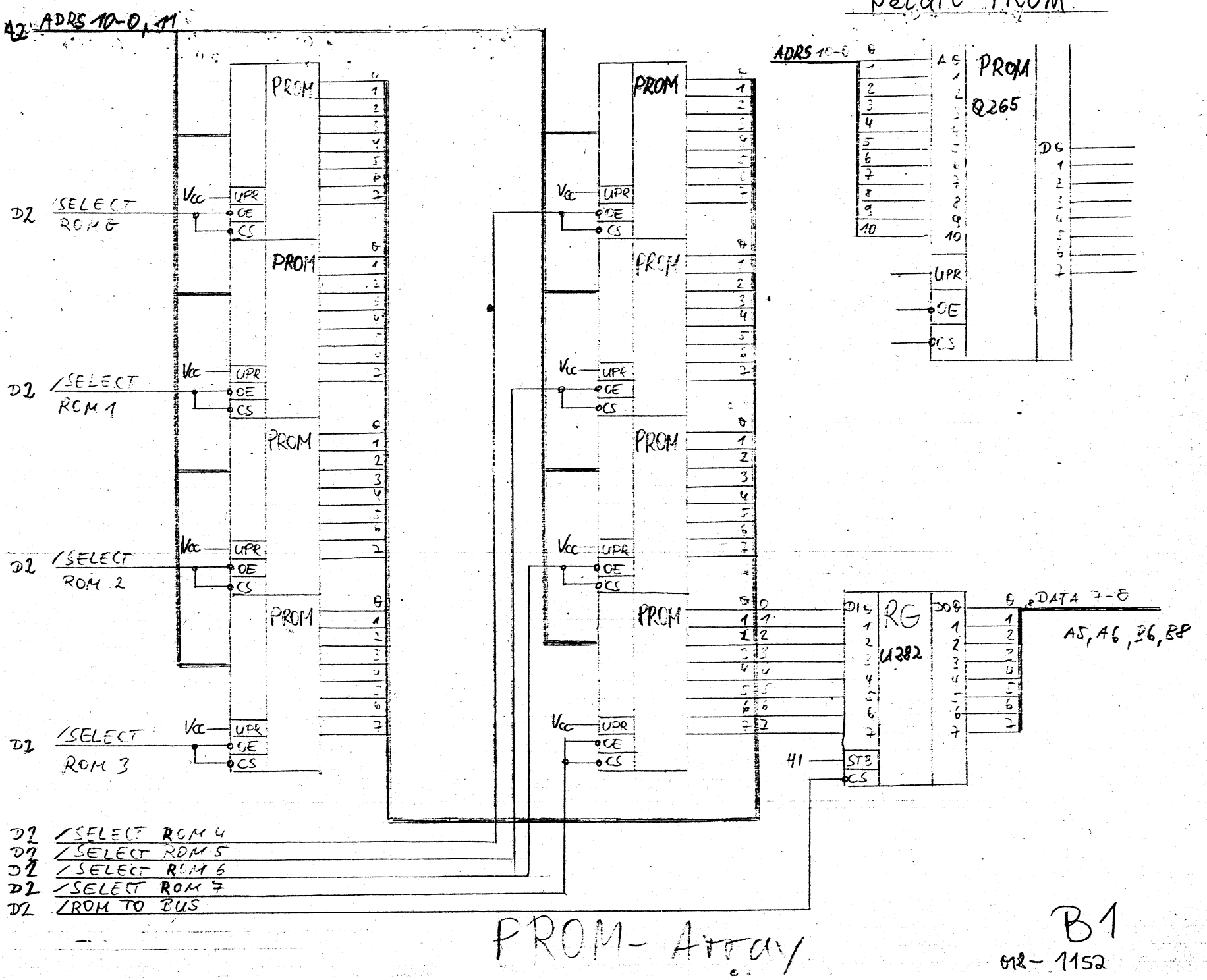
Datenbuskopplung CPU und Bussystem

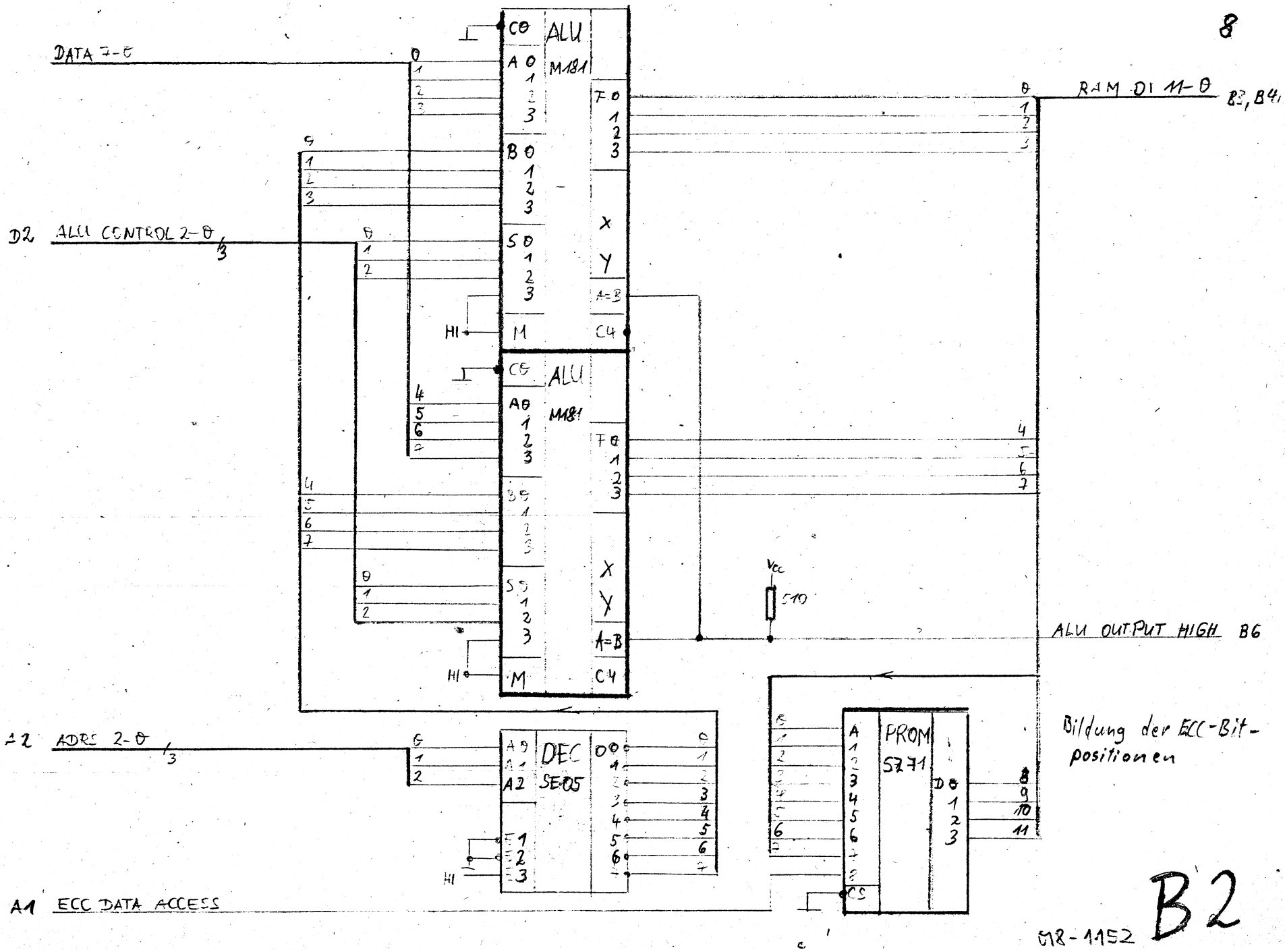
018-1152

A5

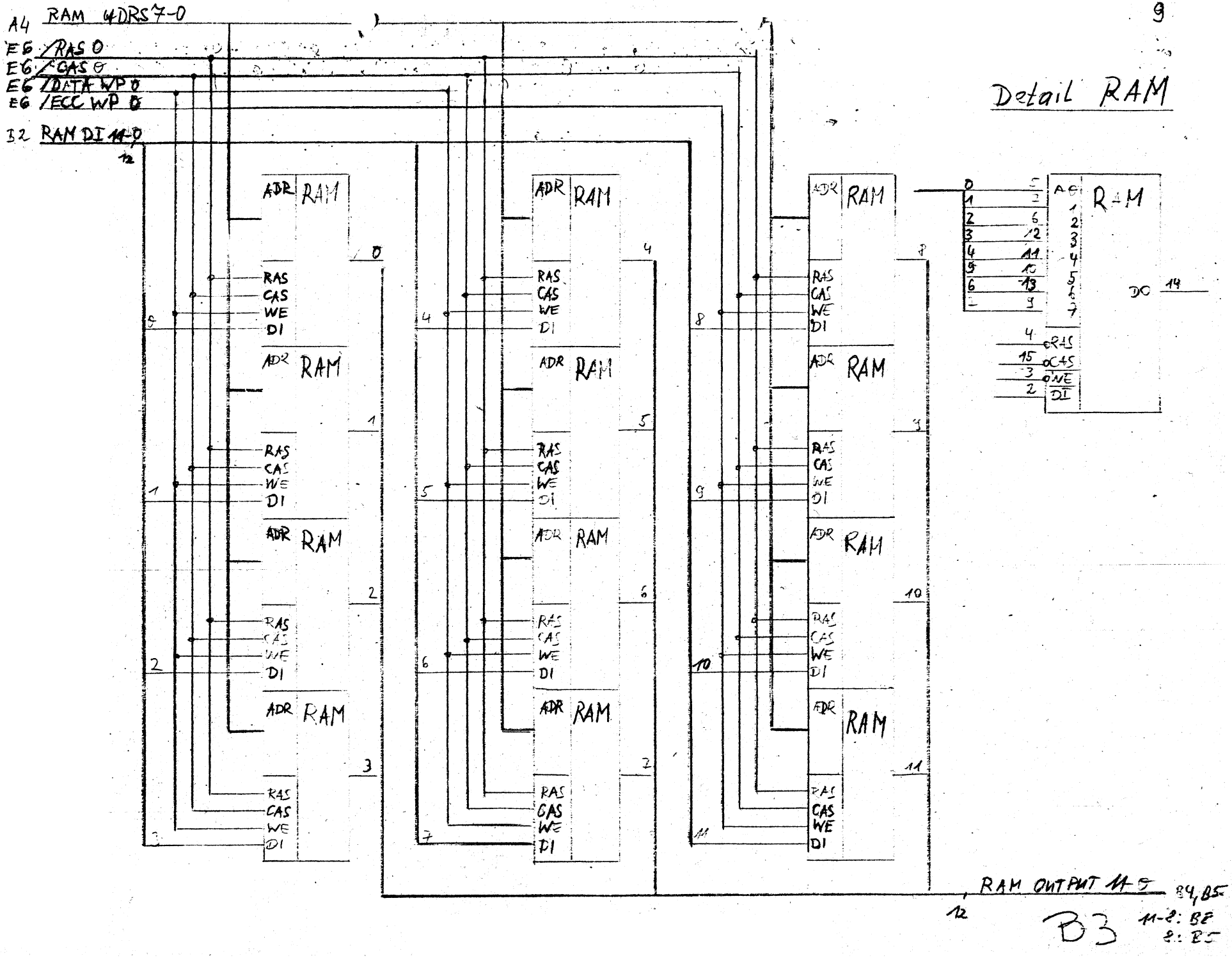

A4 READ INFO 0
C6 DIAG SELECT 0
A3 READ INFO 1
C5 DIAG SELECT 1
+2 READ INFO 2
C4 DIAG SELECT 2
A1 READ INFO 3
A2 DIAG SPIF WRITE
C10 READ INFO 4
D5 DIAG PULSE LATCH
C9 READ INFO 5
C1 DIAG STRB
C8 READ INFO 6
C3 RESET LATCH
C7 READ INFO 7
B7 SEG RAM 12
D2 /SPIF TO BUS
D1.B6 /DIAG PLUG PRESENCE
D3 LOAD OUTBOUND SPIF INFO
B7 SEG RAM 11-9
D1 SPIF WRITE CTL
D3 LOAD SPIF SELECT CODE
MUX SY57
MUX SY57
SE 82
SX 74
4,7k
DATA 7-0
A5, B1, B6, B3
B8
WRITE INFO 0 A4
1 A3
2 A2
3 A1
4 C10
5 C9
6 C8
7 C7
SELECT 0 C6
SELECT 1 C5
SELECT 2 C4
SPIF WRITE C3

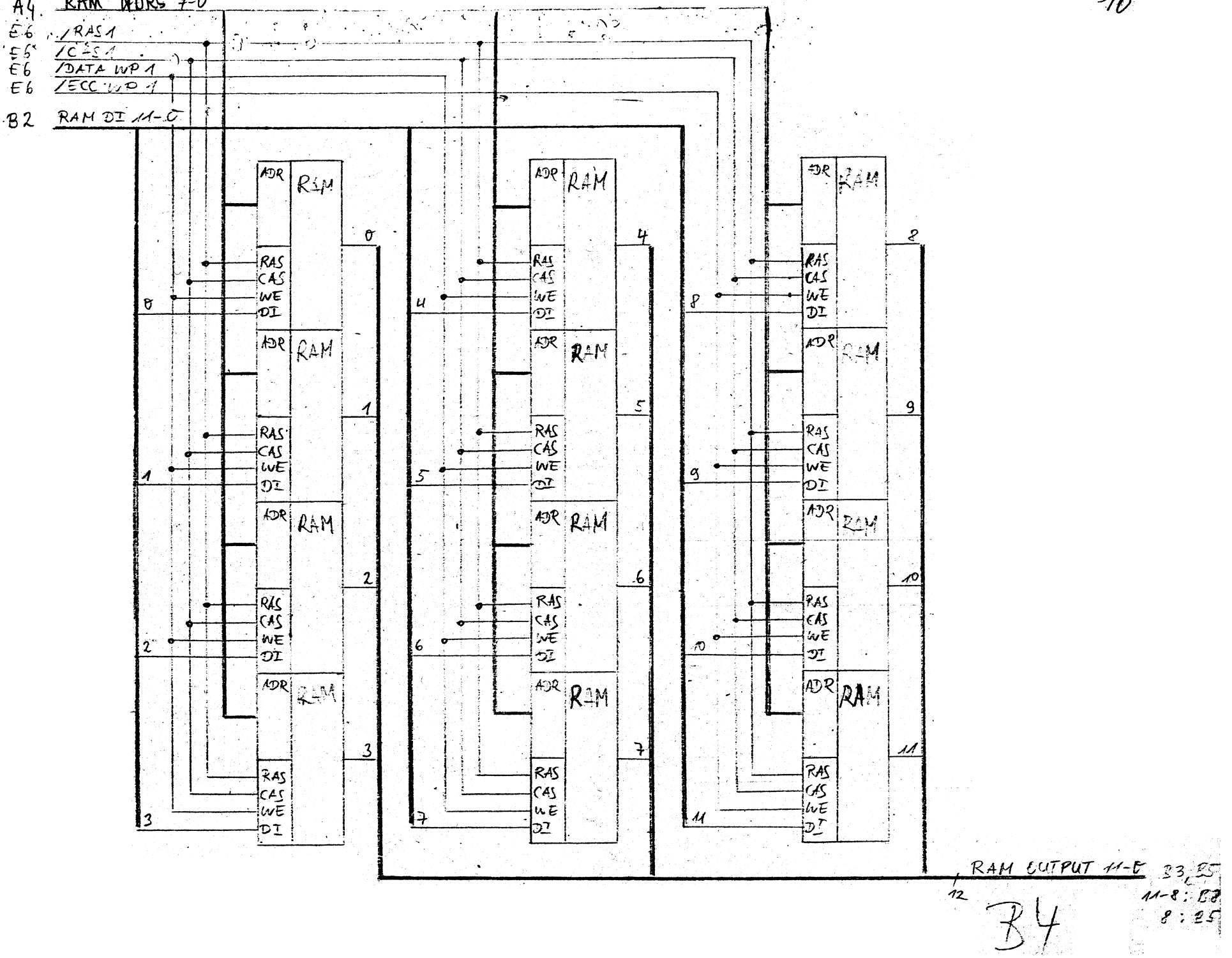
A6

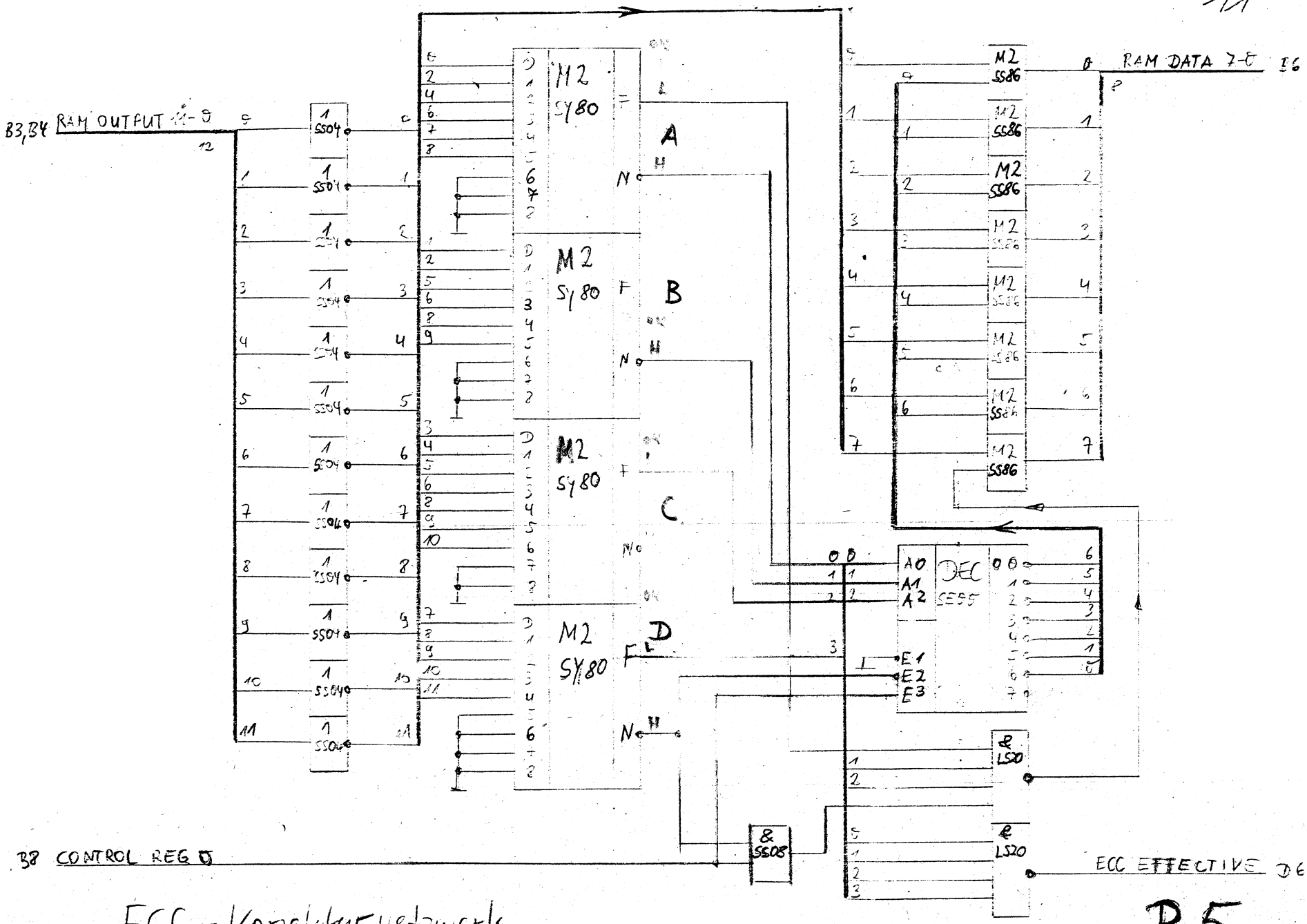

Detail PROM
42 ADRS 10-0, 11
ADRS 10-0
PROM
Q265
D 8
UPR
OE
CS
D2 /SELECT ROM 0
D2 /SELECT ROM 1
D2 /SELECT ROM 2
D2 /SELECT ROM 3
Vcc
RG
U282
DI 8
DO 8
DATA 7-0
A5, A6, B6, B8
41
STB
D2 /SELECT ROM 4
D2 /SELECT ROM 5
D2 /SELECT ROM 6
D2 /SELECT ROM 7
DL /ROM TO BUS
PROM- Array
B1
012-1152


DATA 7-0
D2 ALU CONTROL 2-0
A2 ADRS 2-0
A1 ECC DATA ACCESS
CO ALU M181
A 0 1 2 3
B 0 1 2 3
S 0 1 2 3
M
F 0 1 2 3
X
Y
A=B
C4
HI
CO ALU M181
A0 1 2 3
B 1 2 3
S 1 2 3
M
F 0 1 2 3
X
Y
A=B
C4
HI
DEC SE05
A0 A1 A2
E1 E2 E3
HI
0 1 2 3 4 5 6 7
PROM 5271
A 1 2 3 4 5 6 7 8
CS
D 0 1 2 3
8 9 10 11
RAM DI 11-0 B3, B4
Vcc
510
ALU OUTPUT HIGH B6
Bildung der ECC-Bit-positionen
M8-1152
B2

Detail RAM

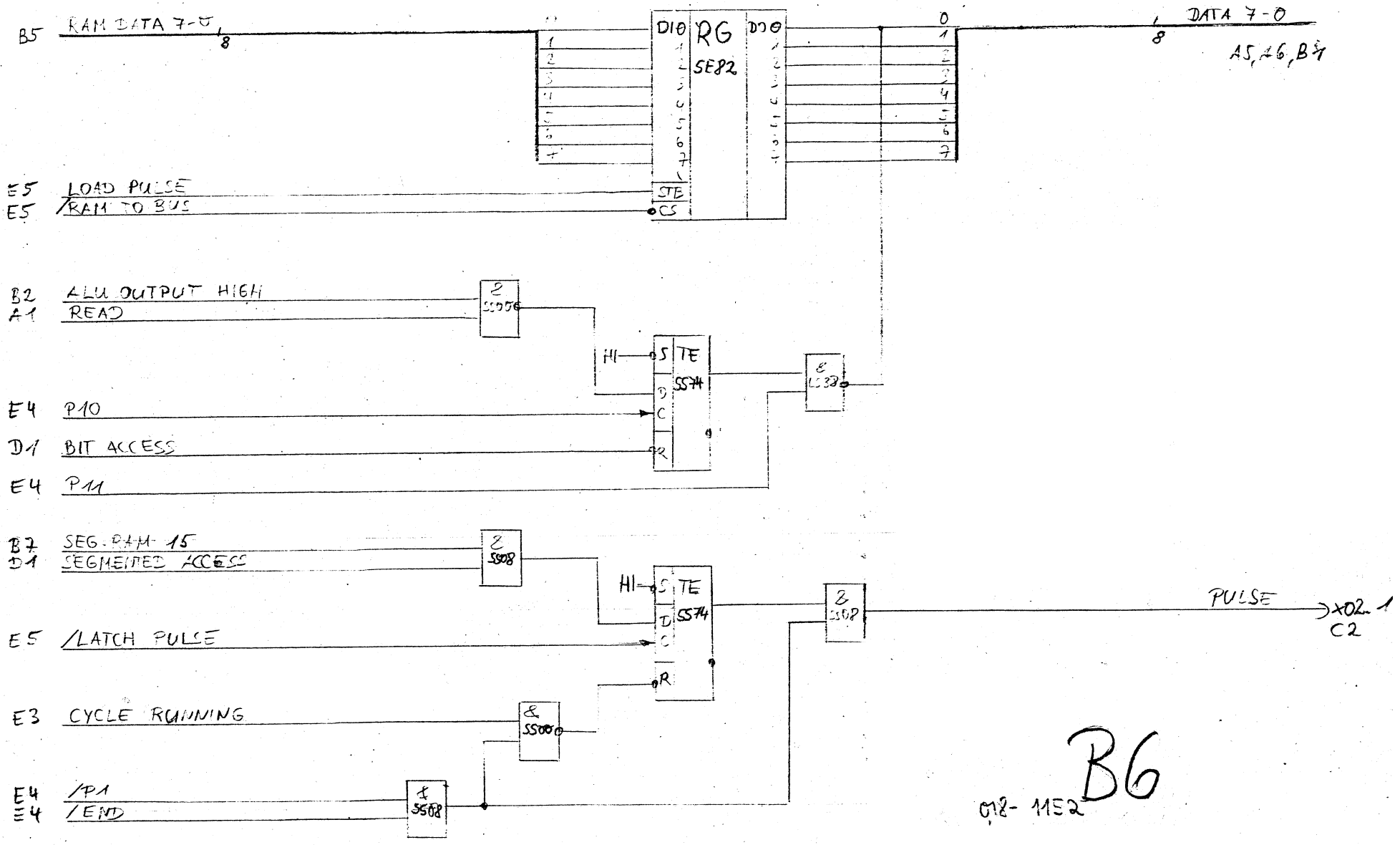

A4 RAM 4DRS7-0
E6 /RAS 0
E6 /CAS 0
E6 /DATA WP 0
E6 /ECC WP 0
B2 RAM DI 11-0
12
ADR
RAM
RAS
CAS
WE
DI
DO
14
RAM OUTPUT 11-0
84,85
B3
11-2: BE
2: B5

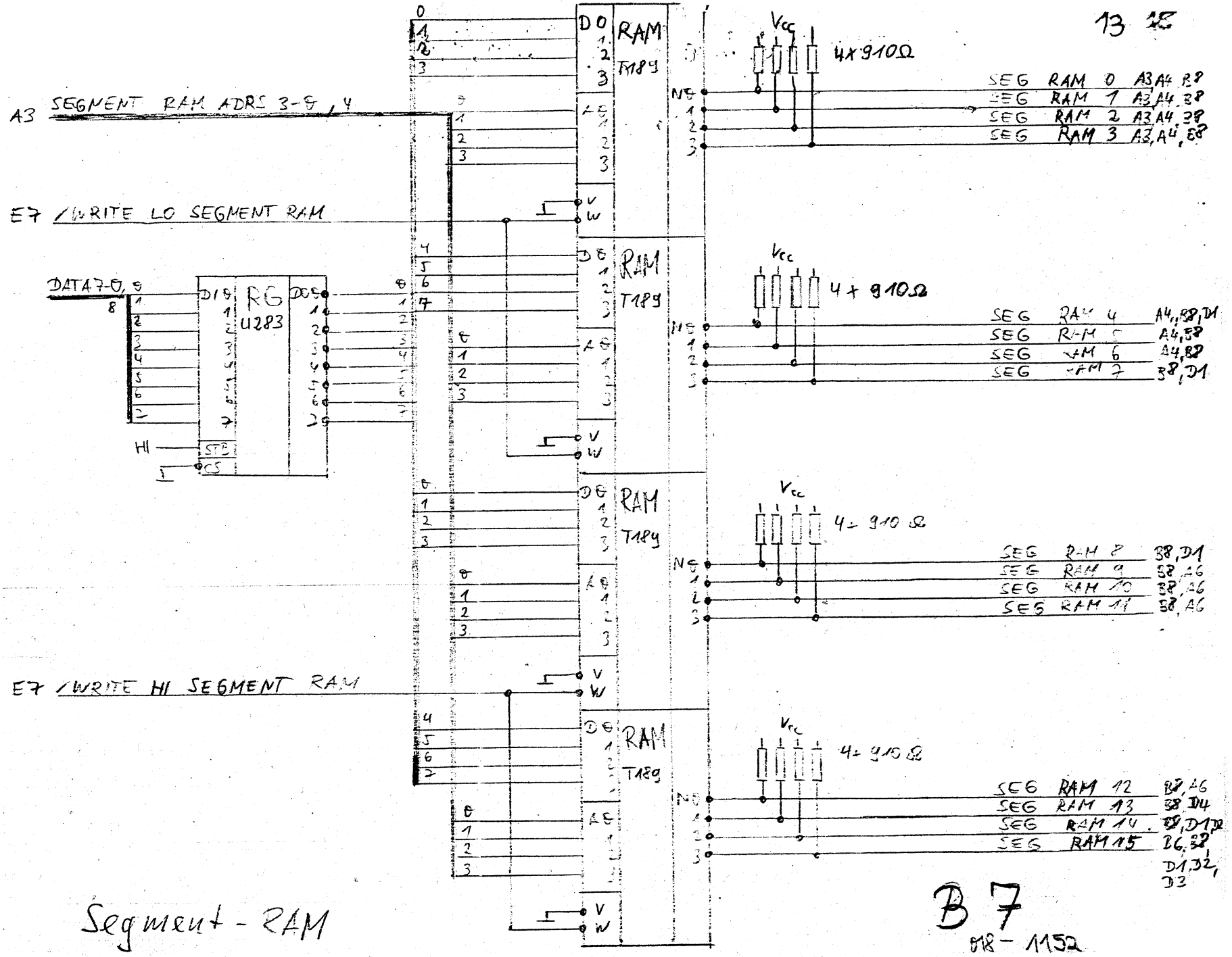

A4 RAM WDRS 4-0
E6 /RAS 1
E6 /CAS 1
E6 /DATA WP 1
E6 /ECC WD 1
B2 RAM DI 11-0
ADR
RAM
RAS
CAS
WE
DI
0
1
2
3
4
5
6
7
8
9
10
11
12
RAM OUTPUT 11-0
B4



ECC - Korrekturnetzwerk

B5

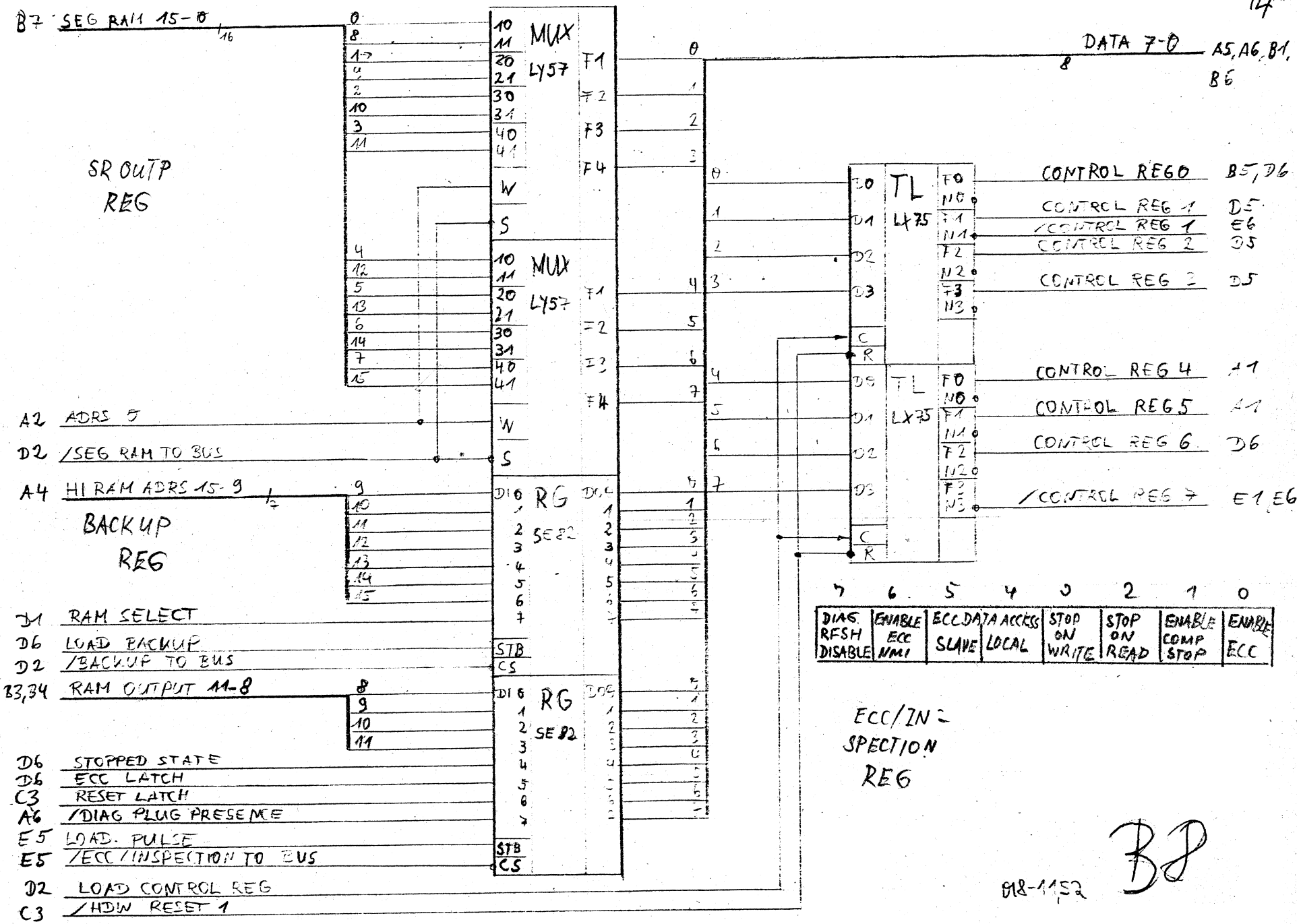

B5 RAM DATA 7-0
8
DIO RG DIO
SE82
STE
CS
0 1 2 3 4 5 6 7
DATA 7-0
8
A5, A6, B4
E5 LOAD PULSE
E5 /RAM TO BUS
B2 ALU OUTPUT HIGH
A1 READ
2 SS08
HI
S TE
D SS74
C
R
& LS32
E4 P10
D1 BIT ACCESS
E4 P11
B7 SEG. RAM 15
D1 SEGMENTED ACCESS
2 SS08
HI
S TE
D SS74
C
R
& SS08
PULSE
x02-1
C2
E5 /LATCH PULSE
E3 CYCLE RUNNING
& SS00
E4 /P1
E4 /END
1 SS08
012-11E2
B6

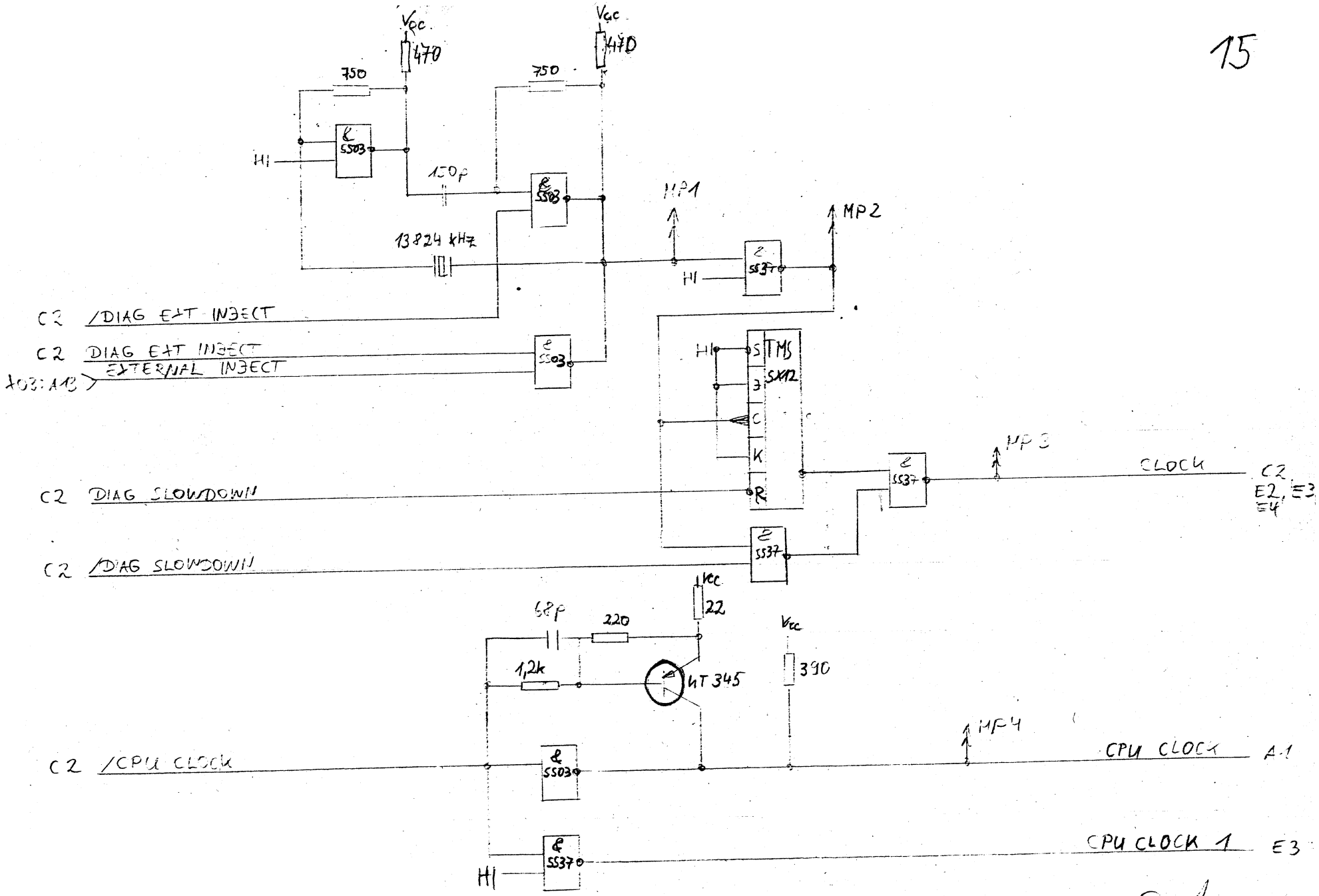


Segment - RAM

B7

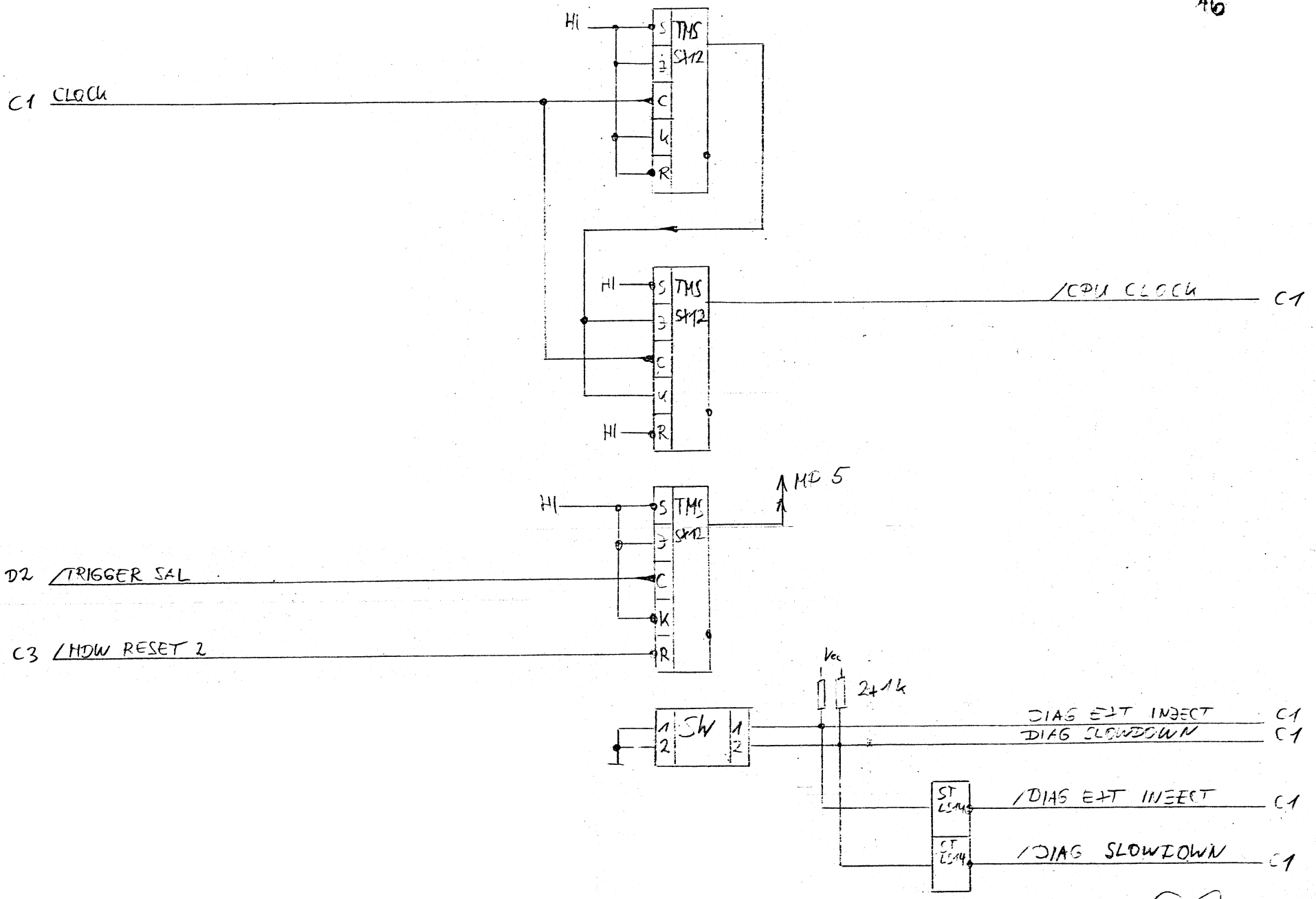
BB - 1152

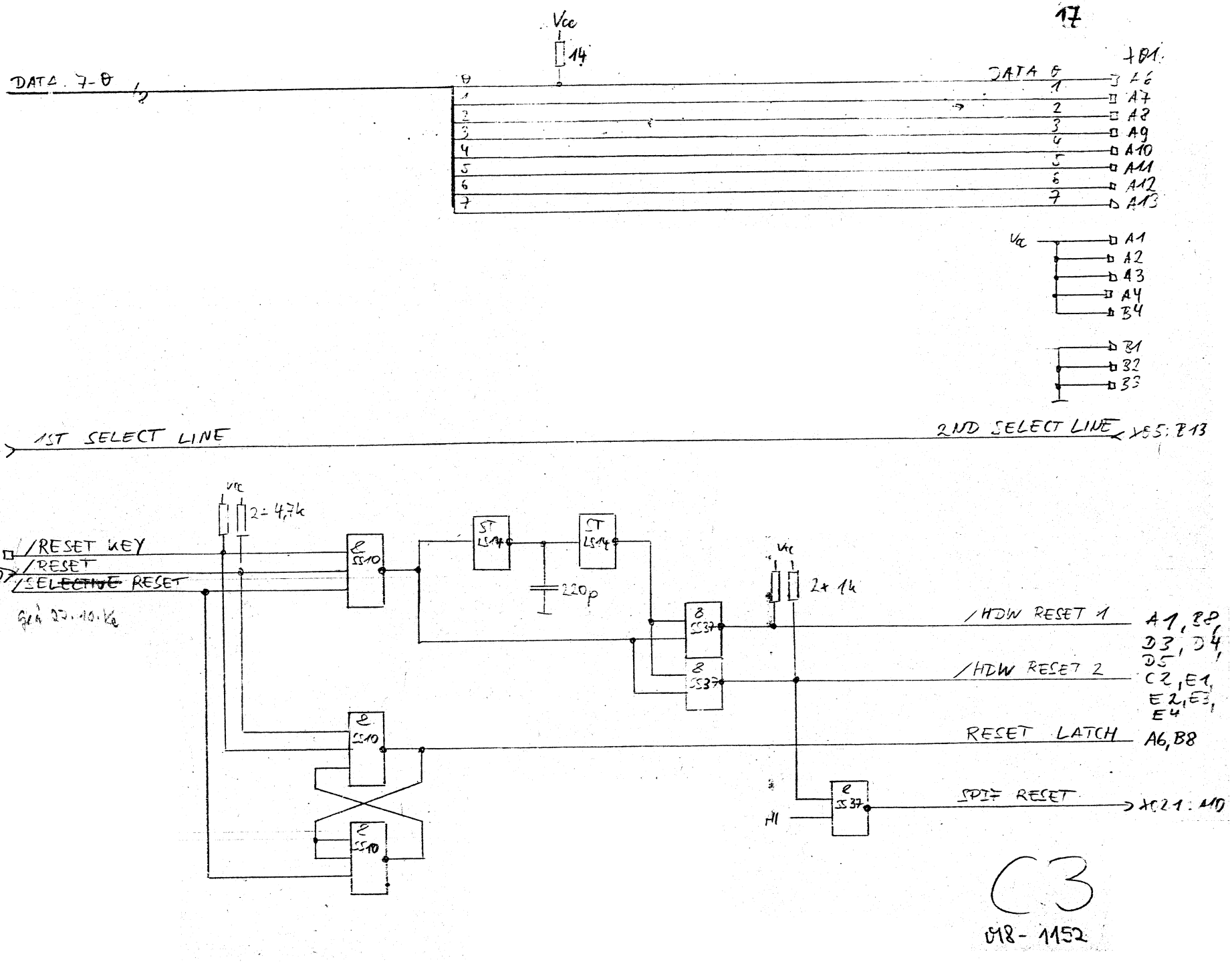

B7 SEG RAM 15-0
SR OUTP REG
A2 ADRS 5
D2 /SEG RAM TO BUS
A4 HI RAM ADRS 15-9
BACK UP REG
D1 RAM SELECT
D6 LOAD BACKUP
D2 /BACKUP TO BUS
B3,B4 RAM OUTPUT 11-8
D6 STOPPED STATE
D6 ECC LATCH
C3 RESET LATCH
A6 /DIAG PLUG PRESENCE
E5 LOAD. PULSE
E5 /ECC/INSPECTION TO BUS
D2 LOAD CONTROL REG
C3 /HDW RESET 1
MUX LY57
RG SE82
DATA 7-0
A5,A6,B1,B6
TL LX75
CONTROL REG0 B5,D6
CONTROL REG 1 D5
/CONTROL REG 1 E6
CONTROL REG 2 D5
CONTROL REG 3 D5
CONTROL REG 4 A1
CONTROL REG 5 A1
CONTROL REG 6 D6
/CONTROL REG 7 E1,E6
7 6 5 4 3 2 1 0
DIAG. RESH DISABLE
ENABLE ECC NMI
ECC DATA SLAVE
ACCESS LOCAL
STOP ON WRITE
STOP ON READ
ENABLE COMP STOP
ENABLE ECC
ECC/INSPECTION REG


Vcc
470
750
Hi
5503
150p
13824 kHz
MP1
MP2
5537
C2 /DIAG EXT INJECT
C2 DIAG EXT INJECT
EXTERNAL INJECT
A03:A13
TMS
SX12
S
J
C
K
R
MP3
CLOCK
C2
E2, E3
E4
C2 DIAG SLOWDOWN
C2 /DIAG SLOWDOWN
68p
220
22
1,2k
HT 345
390
MP4
C2 /CPU CLOCK
CPU CLOCK
A-1
CPU CLOCK 1
E3

C1

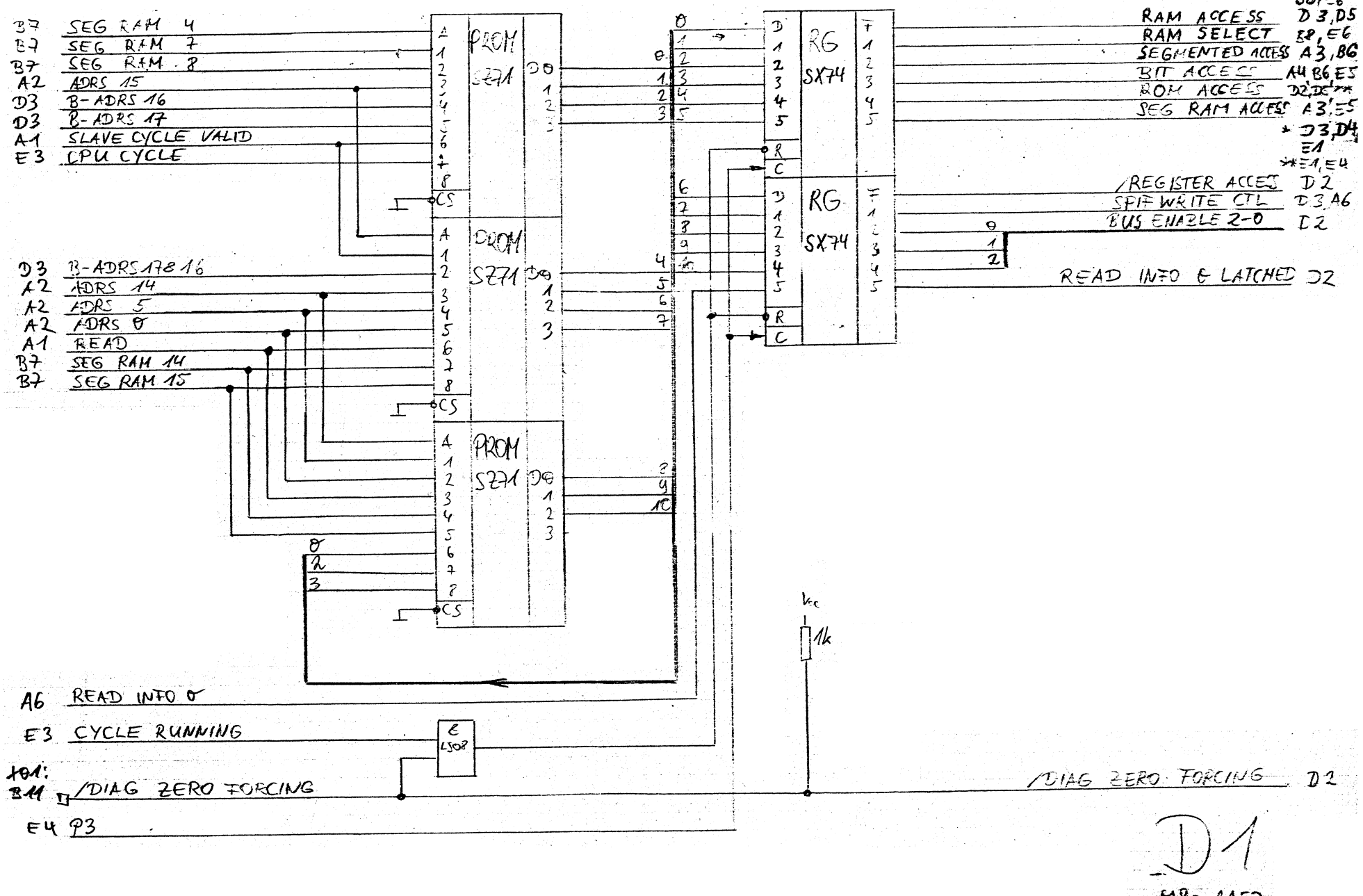
018-1152


HI
S
TMS
SM12
J
C
K
R
C1 CLOCK
HI
/CPU CLOCK
C1
MD 5
D2 /TRIGGER SAL
C3 /MDW RESET 2
Vcc
2+14
SW
1
2
DIAG EJT INJECT
DIAG SLOWDOWN
/DIAG EJT INJECT
/DIAG SLOWDOWN
C1
C2


Vcc
14
DATA 7-0
0
1
2
3
4
5
6
7
J01
DATA 0
1
2
3
4
5
6
7
A6
A7
A8
A9
A10
A11
A12
A13
Vcc
A1
A2
A3
A4
B4
B1
B2
B3
J05:A1
1ST SELECT LINE
2ND SELECT LINE
J05:B13
Vcc
2x 4,7k
J01:B7
/RESET KEY
J04:B10
/RESET
/SELECTIVE RESET
E2
Gnd
220p
2x 1k
/HDW RESET 1
A1, B2, D3, D4, D5,
/HDW RESET 2
C2, E1, E2, E3, E4
RESET LATCH
A6, B8
SPI RESET
J021:A10
HI

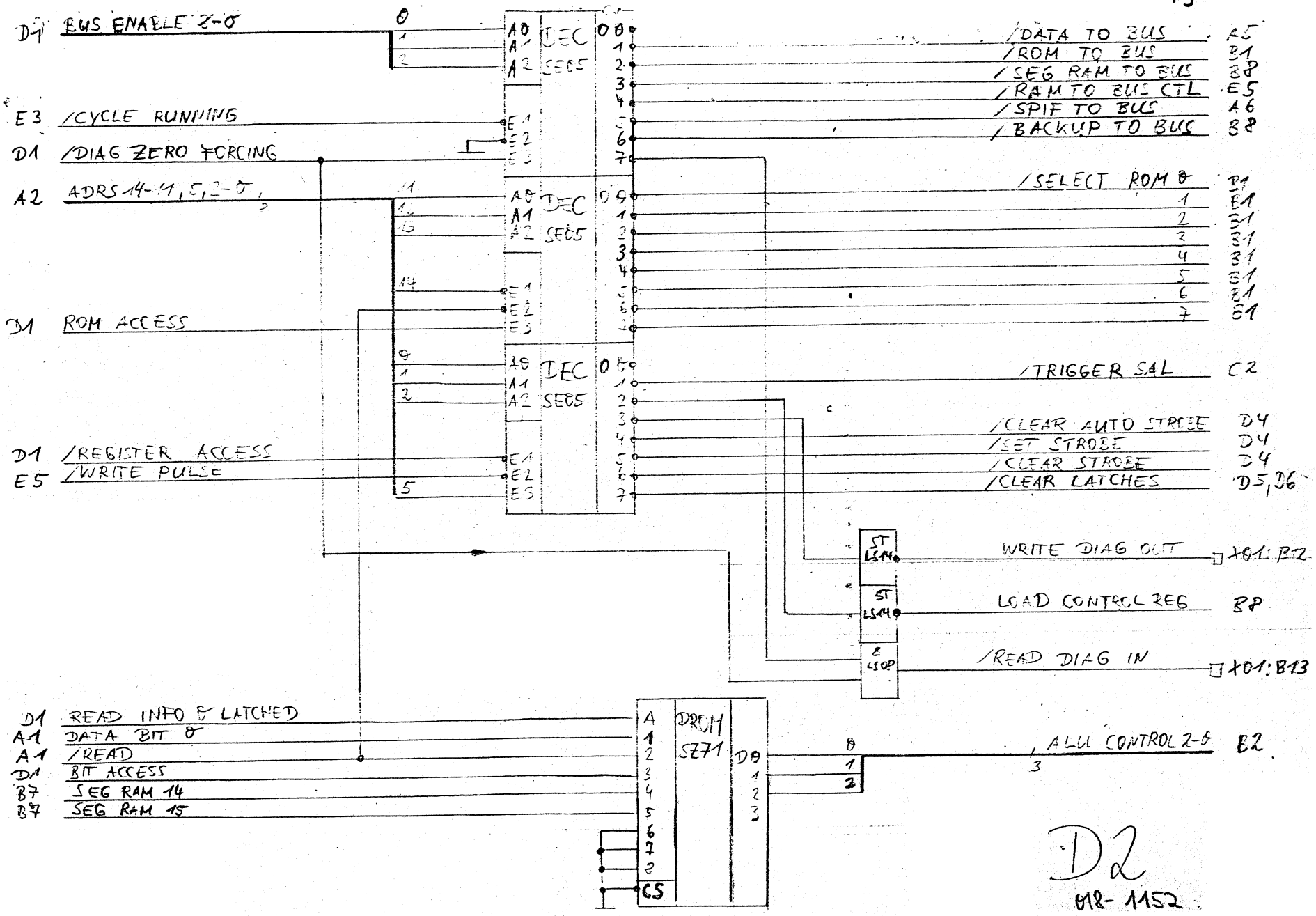
C3

018-1152


B7 SEG RAM 4
B7 SEG RAM 7
B7 SEG RAM 8
A2 ADRS 15
D3 B-ADRS 16
D3 B-ADRS 17
A1 SLAVE CYCLE VALID
E3 CPU CYCLE
PROM S271
CS
D3 B-ADRS 17 & 16
A2 ADRS 14
A2 ADRS 5
A2 ADRS 0
A1 READ
B7 SEG RAM 14
B7 SEG RAM 15
RG SX74
RAM ACCESS D3,D5
RAM SELECT E8,E6
SEGMENTED ACCESS A3,B6
BIT ACCESS A4,B6,E5
ROM ACCESS D2,D6*,**
SEG RAM ACCESS A3,E5
* D3,D4 E1
** E1,E4
/REGISTER ACCESS D2
SPI WRITE CTL D3,A6
BUS ENABLE 2-0 D2
READ INFO 0 LATCHED D2
A6 READ INFO 0
E3 CYCLE RUNNING
/DIAG ZERO FORCING
E4 P3
/DIAG ZERO FORCING D2
1k

D1

E18-1152


D1 BUS ENABLE 2-0
E3 /CYCLE RUNNING
D1 /DIAG ZERO FORCING
A2 ADRS 14-11, 5, 2-0,
D1 ROM ACCESS
D1 /REGISTER ACCESS
E5 /WRITE PULSE
D1 READ INFO & LATCHED
A1 DATA BIT 0
A1 /READ
D1 BIT ACCESS
B7 SEG RAM 14
B7 SEG RAM 15
DEC SEL5
DROM S271
/DATA TO BUS A5
/ROM TO BUS B1
/SEG RAM TO BUS B8
/RAM TO BUS CTL E5
/SPIF TO BUS A6
/BACKUP TO BUS B8
/SELECT ROM 0 B1
1 E1
2 E1
3 B1
4 B1
5 C1
6 B1
7 C1
/TRIGGER SAL C2
/CLEAR AUTO STROBE D4
/SET STROBE D4
/CLEAR STROBE D4
/CLEAR LATCHES D5,D6
WRITE DIAG OUT
LOAD CONTROL REG B8
/READ DIAG IN
ALU CONTROL 2-0 B2
D2
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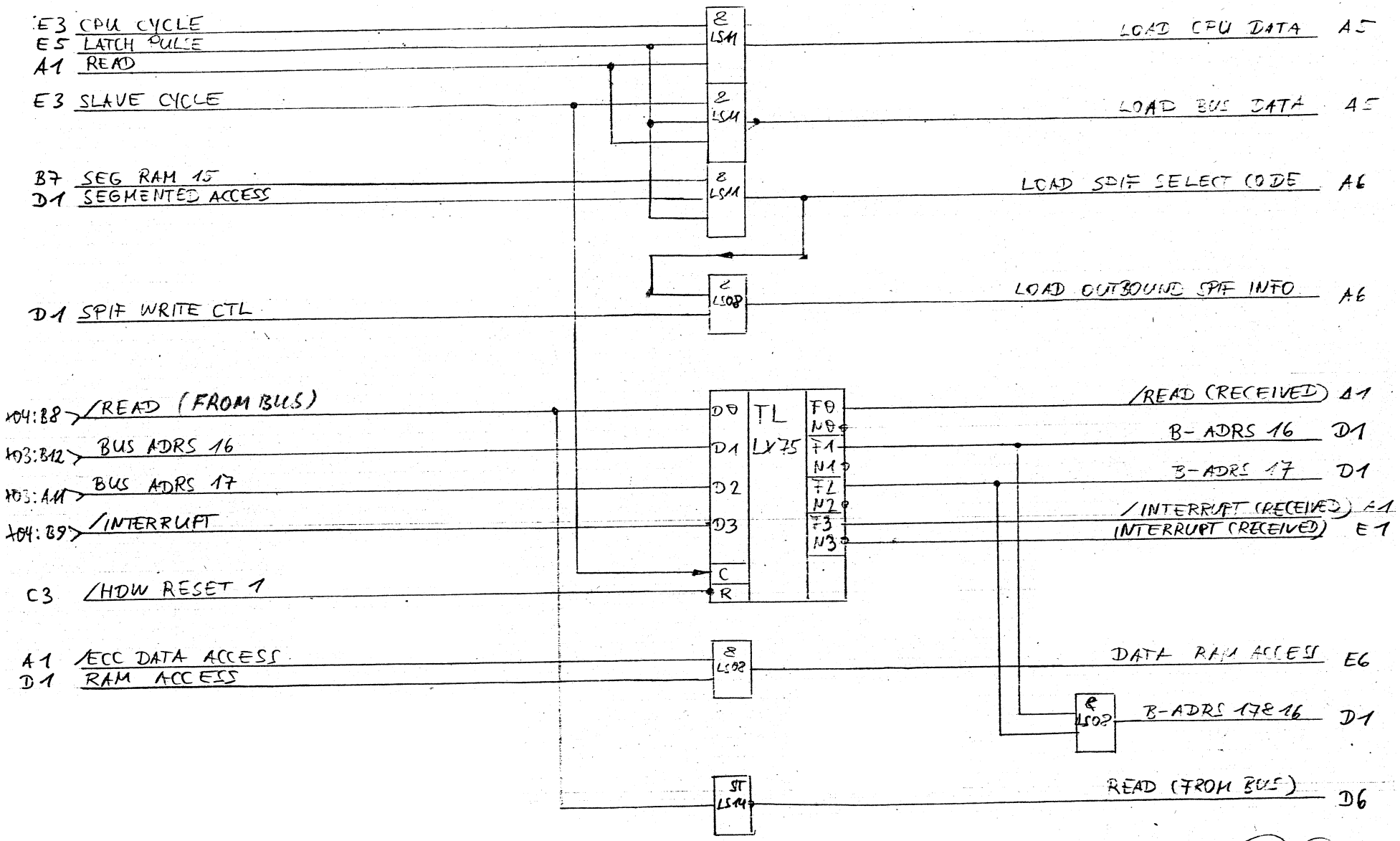
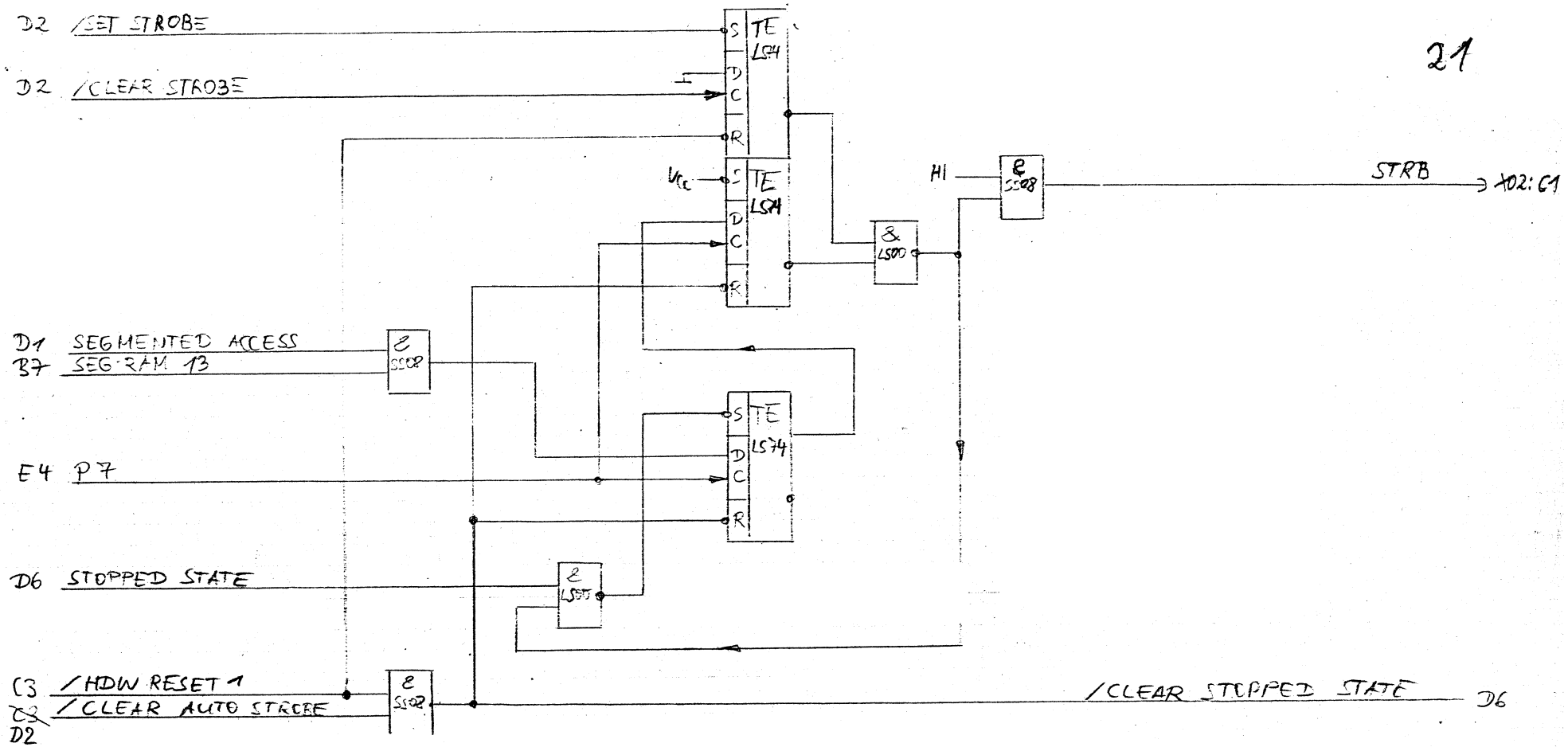

E3 CPU CYCLE
E5 LATCH PULSE
A1 READ
E3 SLAVE CYCLE
B7 SEG RAM 15
D1 SEGMENTED ACCESS
D1 SPIF WRITE CTL
H04:B8 /READ (FROM BUS)
H03:B12 BUS ADRS 16
H03:A11 BUS ADRS 17
H04:B9 /INTERRUPT
C3 /HDW RESET 1
A1 /ECC DATA ACCESS
D1 RAM ACCESS
LOAD CPU DATA A5
LOAD BUS DATA A5
LOAD SPIF SELECT CODE A6
LOAD OUTBOUND SPIF INFO A6
/READ (RECEIVED) A1
B-ADRS 16 D1
B-ADRS 17 D1
/INTERRUPT (RECEIVED) A1
INTERRUPT (RECEIVED) E1
DATA RAM ACCESS E6
B-ADRS 17&16 D1
READ (FROM BUS) D6
LS14
LS08
LS02
TL
LY75


D2 /SET STROBE
D2 /CLEAR STROBE
S
D
C
R
TE
LS74
V_{cc}
HI
&
LS00
STRB
A02: C1
D1 SEGMENTED ACCESS
B7 SEG-RAM 13
LS08
E4 P7
LS74
D6 STOPPED STATE
LS05
C3 /HDW RESET 1
C3 /CLEAR AUTO STROBE
D2
/CLEAR STOPPED STATE
D6

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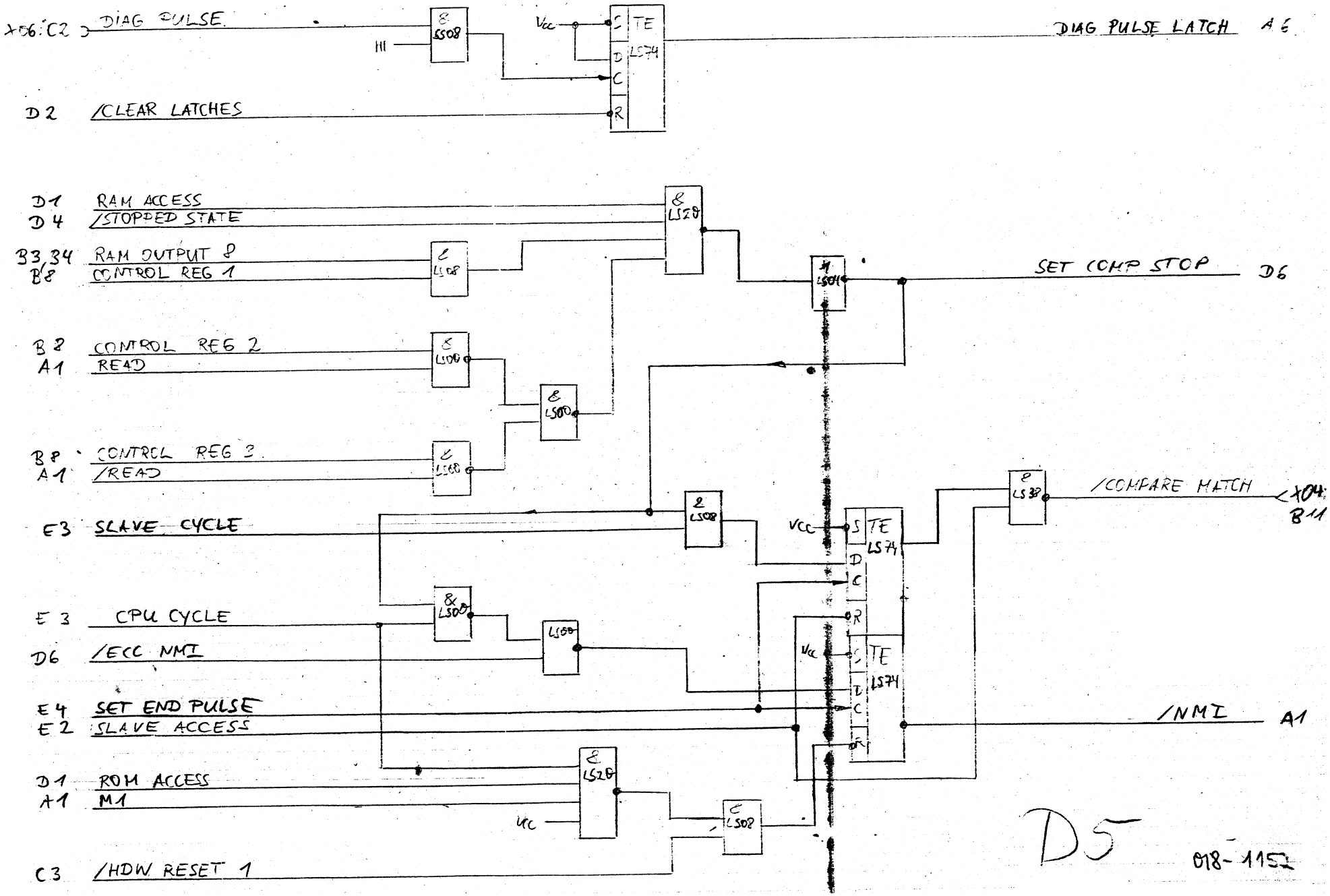
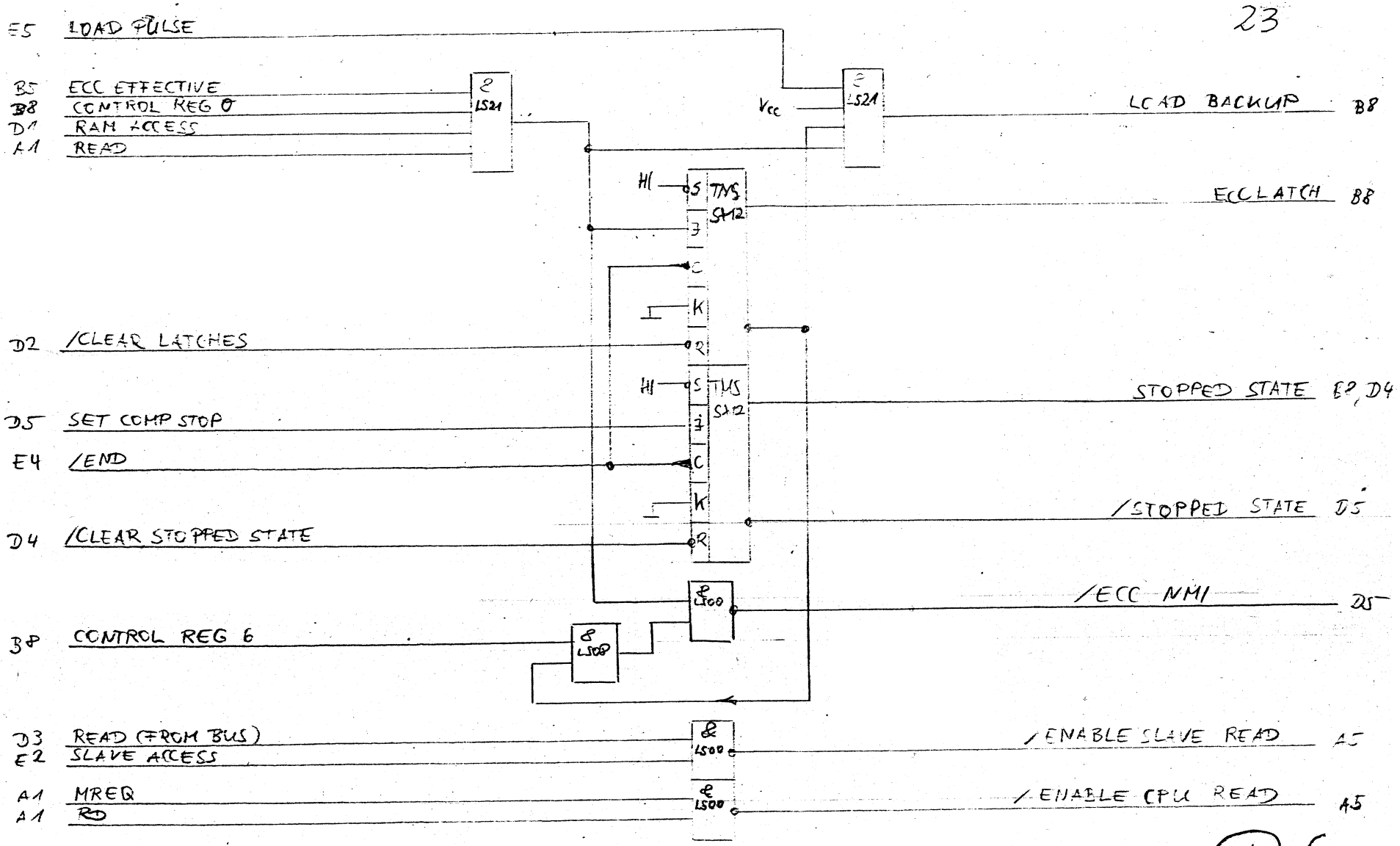
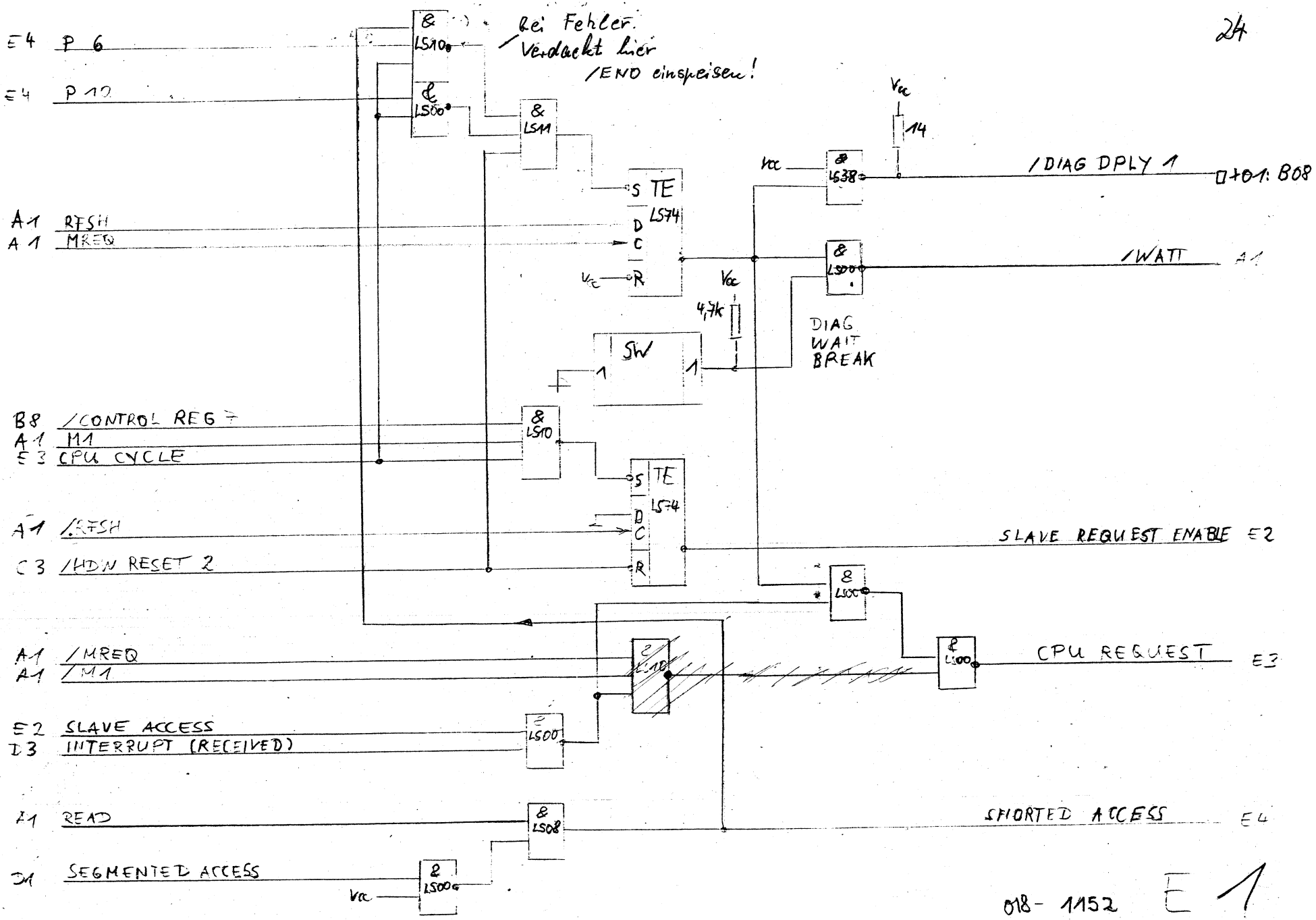
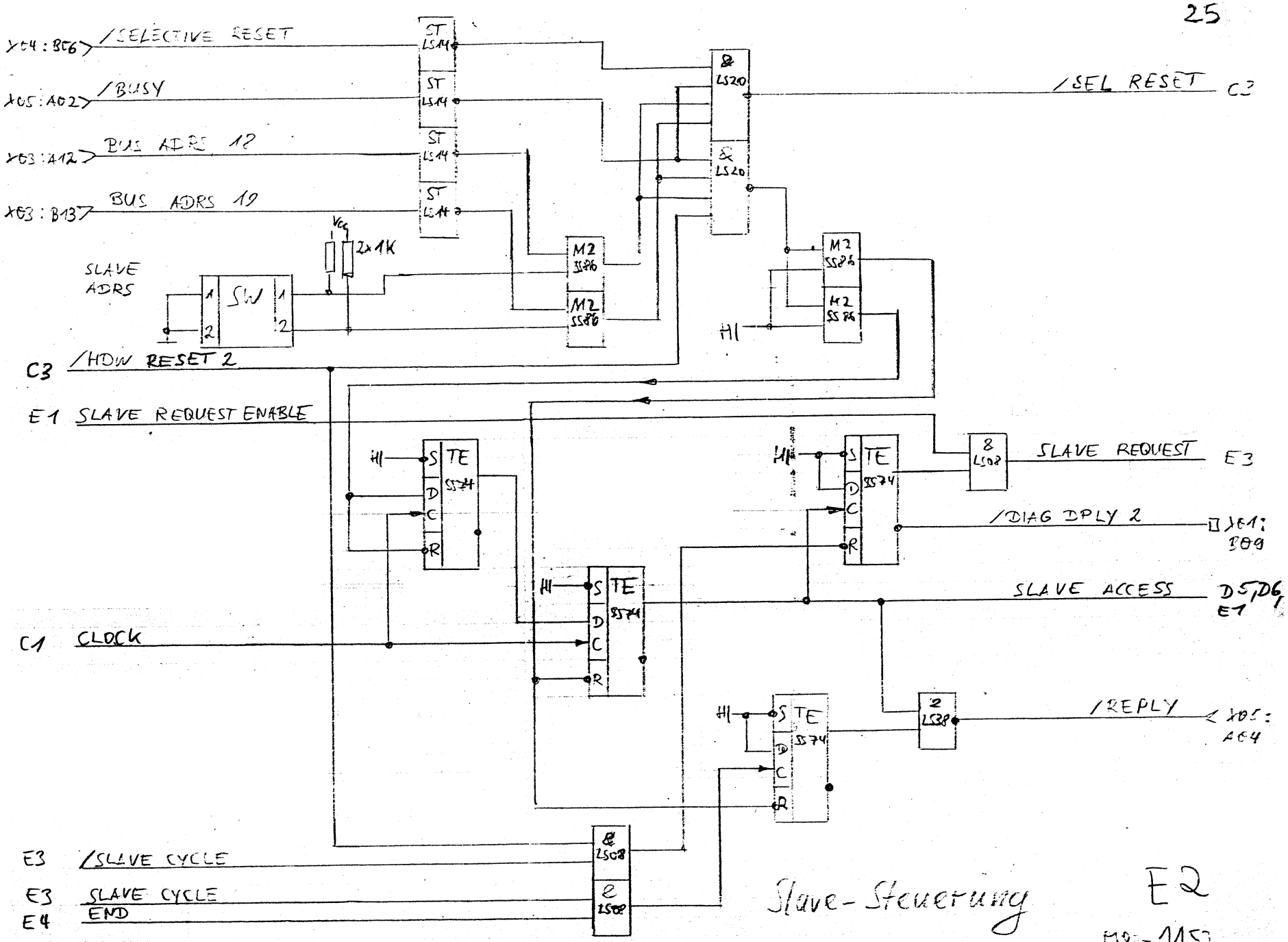

X06:C2
DIAG PULSE
HI
&
LS08
Vcc
S
D
C
R
TE
LS74
DIAG PULSE LATCH
A6
D2
/CLEAR LATCHES
D1
RAM ACCESS
D4
/STOPPED STATE
&
LS20
B3,B4
B8
RAM OUTPUT 8
CONTROL REG 1
LS08
LS04
SET COMP STOP
D6
B8
A1
CONTROL REG 2
READ
LS00
B8
A1
CONTROL REG 3
/READ
E3
SLAVE CYCLE
LS32
/COMPARE MATCH
X04:
B11
E3
CPU CYCLE
D6
/ECC NMI
LS86
E4
E2
SET END PULSE
SLAVE ACCESS
/NMI
A1
D1
A1
ROM ACCESS
M1
C3
/HDW RESET 1
D5
018-1152

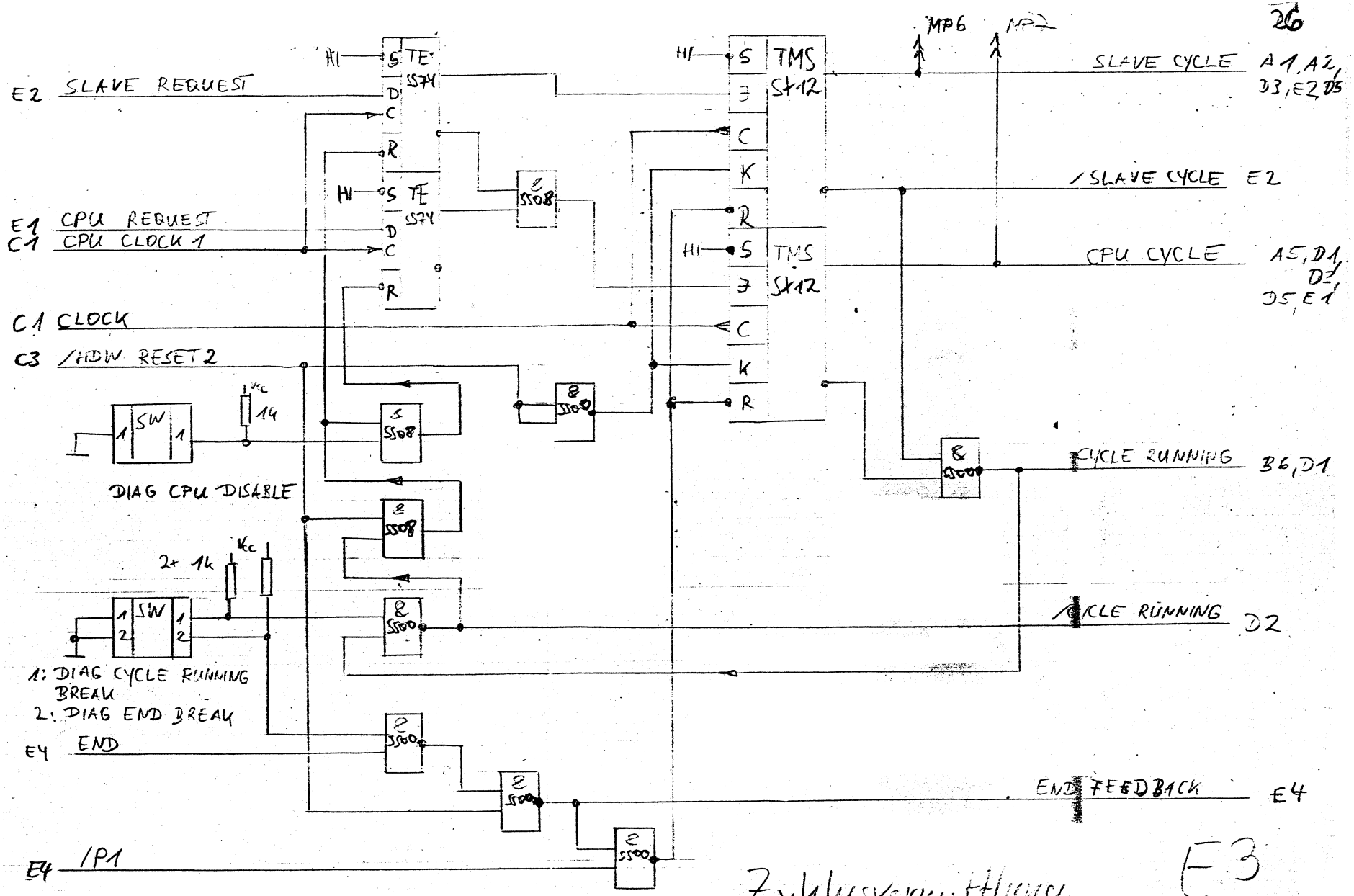

E5 LOAD PULSE
B5 ECC EFFECTIVE
B8 CONTROL REG 0
D1 RAM ACCESS
A1 READ
8 LS21
Vcc
8 LS21
LOAD BACKUP B8
HI
5 TMS
3 SM12
ECCLATCH B8
C
K
D2 /CLEAR LATCHES
R
HI
S TMS
J SM12
STOPPED STATE E?, D4
D5 SET COMP STOP
E4 /END
C
K
/STOPPED STATE D5
D4 /CLEAR STOPPED STATE
R
8 LS00
/ECC NMI D5
B8 CONTROL REG 6
8 LS08
D3 READ (FROM BUS)
E2 SLAVE ACCESS
8 LS00
/ENABLE SLAVE READ A5
A1 MREQ
A1 RD
8 LS00
/ENABLE CPU READ A5

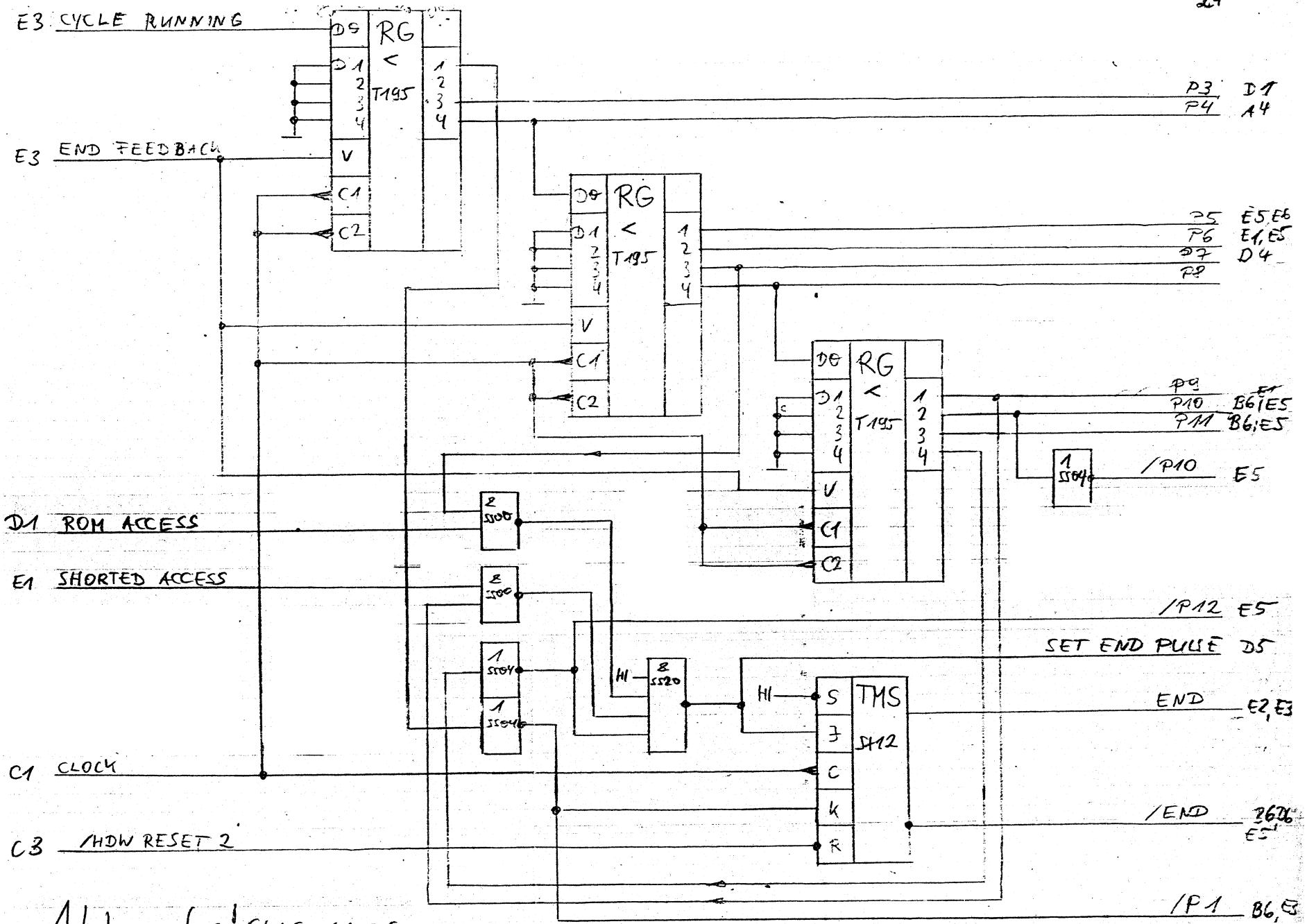
D6

018-1152


E4 P 6
E4 P 10
bei Fehler: Verdrahtet hier /END einspeisen!
A1 RFSH
A1 MREQ
B8 /CONTROL REG 7
A1 M1
E3 CPU CYCLE
A1 /RFSH
C3 /HDW RESET 2
A1 /MREQ
A1 /M1
E2 SLAVE ACCESS
D3 INTERRUPT (RECEIVED)
A1 READ
D1 SEGMENTED ACCESS
Vcc
14
4,7k
/DIAG DPLY 1
D+01: B08
/WAIT
A1
DIAG
WAIT
BREAK
SLAVE REQUEST ENABLE E2
CPU REQUEST
E3
SHORTED ACCESS
E4
LS10
LS00
LS11
LS74
LS38
LS04
SW
LS70
LS08
018- 1152
E 1

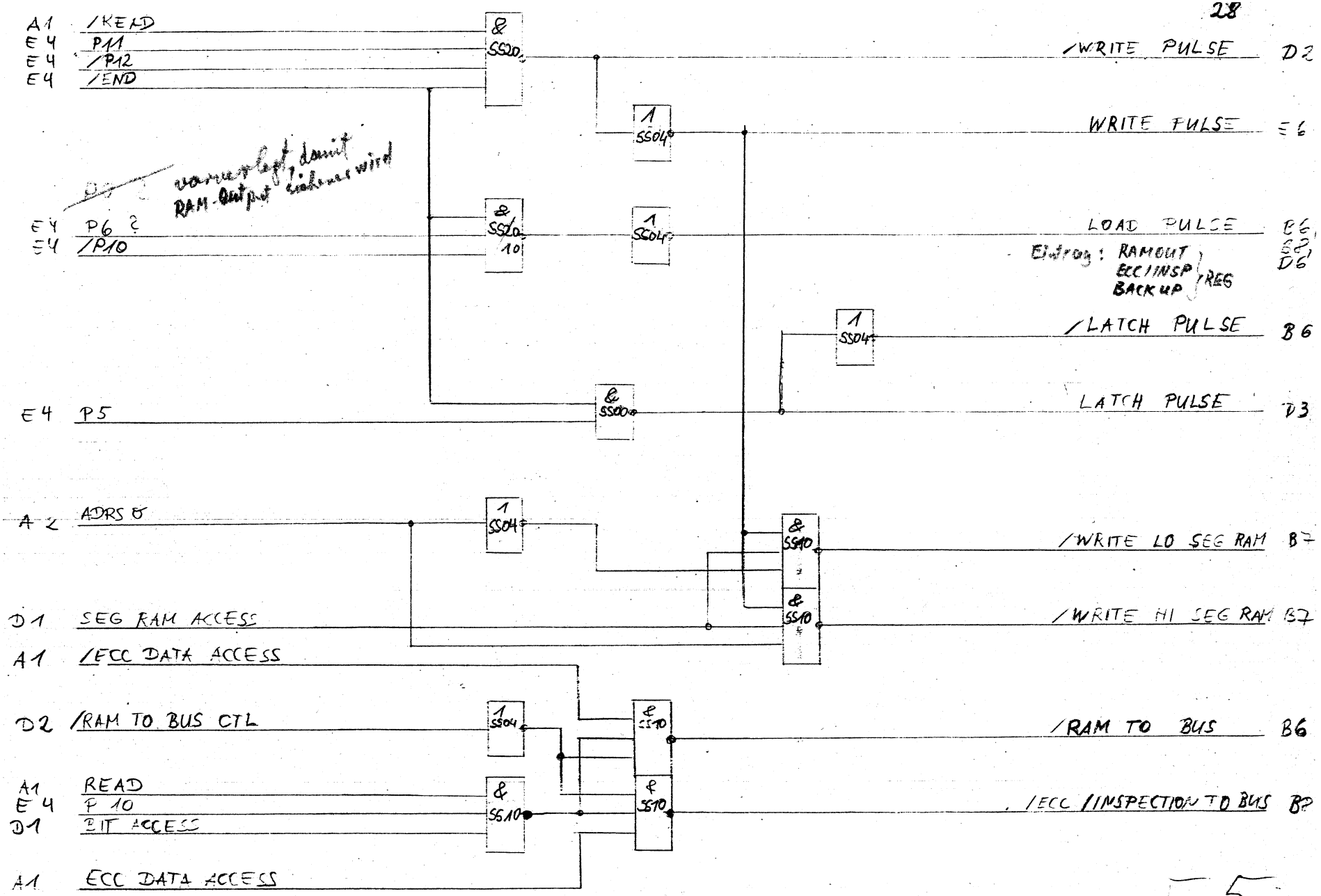

X04 : B06 /SELECTIVE RESET
X05 : A02 /BUSY
X03 : A12 BUS ADRS 12
X03 : B13 BUS ADRS 19
ST LS14
2 LS20
& LS20
/SEL RESET C3
Vcc
2x1K
SLAVE ADRS
SW
M2 SS86
H1
C3 /HDW RESET 2
E1 SLAVE REQUEST ENABLE
S TE SS74
D
C
R
8 LS02
SLAVE REQUEST E3
/DIAG DPLY 2
X01: B09
SLAVE ACCESS D5,D6, E1
C1 CLOCK
2 LS38
/REPLY
X05: A04
& LS08
E3 /SLAVE CYCLE
E3 SLAVE CYCLE
E4 END
Slave-Steuerung
E2
E12-1152


E2 SLAVE REQUEST
E1 CPU REQUEST
C1 CPU CLOCK 1
C1 CLOCK
C3 /HDW RESET 2
DIAG CPU DISABLE
2x 1k
1: DIAG CYCLE RUNNING BREAK
2: DIAG END BREAK
E4 END
E4 /P1
HI
SLAVE CYCLE A1, A2, D3, E2, D5
/SLAVE CYCLE E2
CPU CYCLE A5, D1, D2, D5, E1
CYCLE RUNNING B6, D1
/CYCLE RUNNING D2
END FEEDBACK E4
Zyklussteuerung
E3
818 - 1152



Ablaufsteuerung

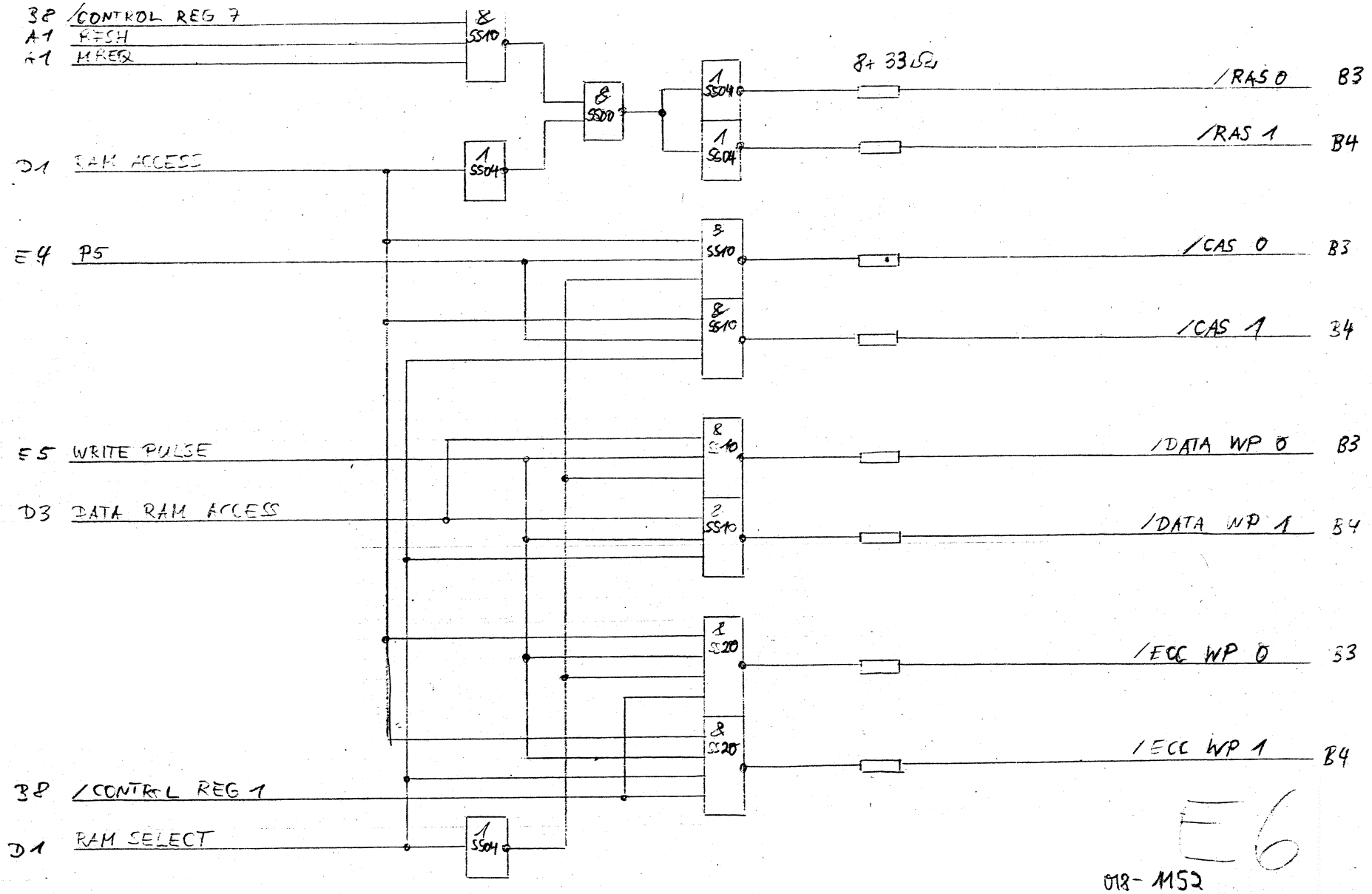
618-1152 E4



ECC/INSPECTION TO BUS = ECC DATA ACCESS & RAM TO BUS CTL & (/READ v /P10 v /B17 ACCESS)

E5

018-1152


B2 /CONTROL REG 7
A1 REFSH
A1 MREQ
D1 RAM ACCESS
E4 P5
E5 WRITE PULSE
D3 DATA RAM ACCESS
B2 /CONTROL REG 1
D1 RAM SELECT
8+ 33Ω
/RAS 0 B3
/RAS 1 B4
/CAS 0 B3
/CAS 1 B4
/DATA WP 0 B3
/DATA WP 1 B4
/ECC WP 0 B3
/ECC WP 1 B4
E6
018-1152