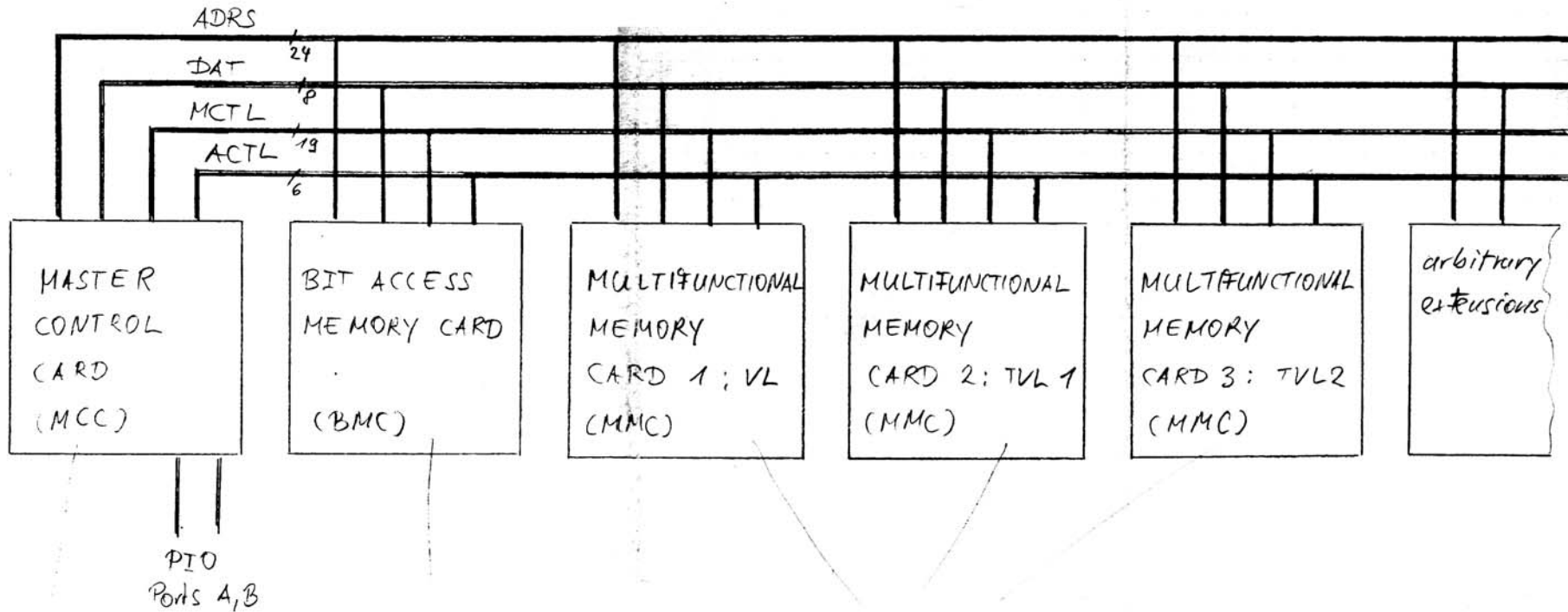


009.A INDUSTRIAL CONTROL SYSTEM OVERVIEW

10.10.85 Clu

1



- CPU
- CTC
- PIO
- 2 k ROM
- 2 k RAM
- SEQUENCER

- 8k RAM
- 16 x 4 bit BIT ADDS
- SEGMENT RAM
- BIT/BYTE-ACCESS LOGIC

- UP TO 128k BYTES MEMORY
- TVL COMPARE LOGIC
- ADRS GENERATOR

- MMC FUNCTIONS
- UNIVERSAL MEMORY
 - VARIABLE LIST MEMORY
 - TVL MEMORY

CONTROL BUS LINES

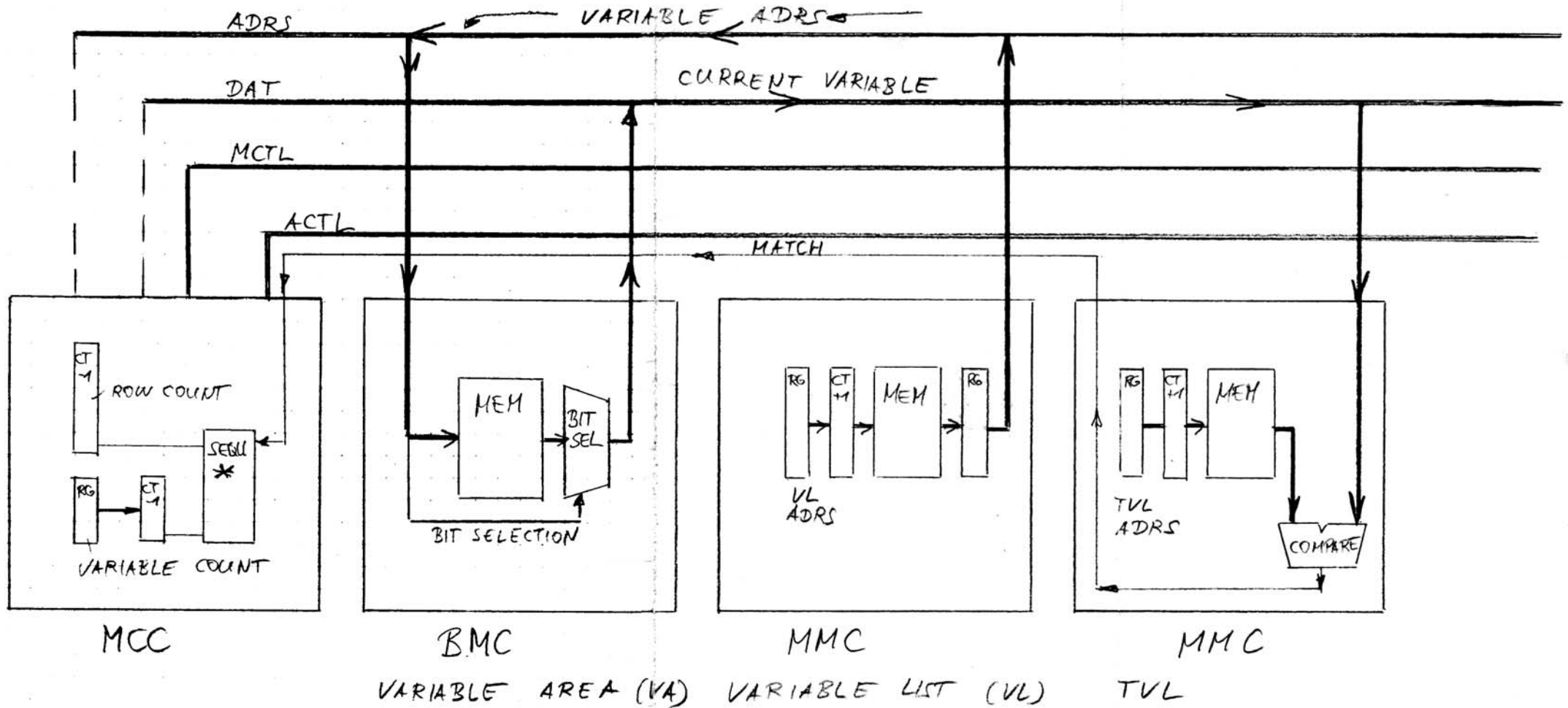
a.) MICROPROCESSOR (MCTL)

- | | | | | | | |
|--------|--------|---------|---------|---------|-------|---------|
| • MREQ | • RD | • BUSRQ | • WAIT | • RESET | • IEI | • MEMDI |
| • IORQ | • WR | • BUSAK | • READY | • INT | • IEO | • IOBI |
| • MA | • RFSH | • HALT | • CLOCK | • NMI | | |

b.) CONTROLLER AUGMENTATION (ACTL)

- MODE 3-0
- STB
- MATCH

009. A COMPARE MODE BASIC INFORMATION FLOW



* steuert:

MREQ, RD

MODE 3-0

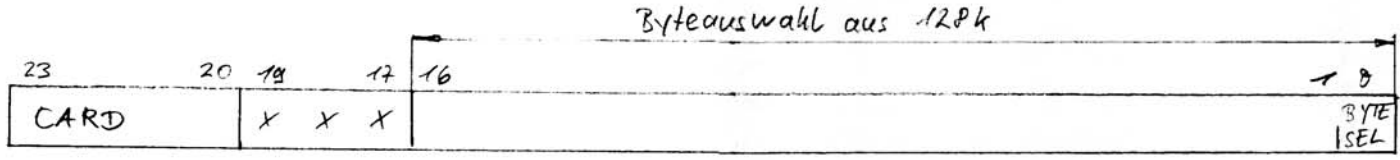
STB

10.10.95 lla

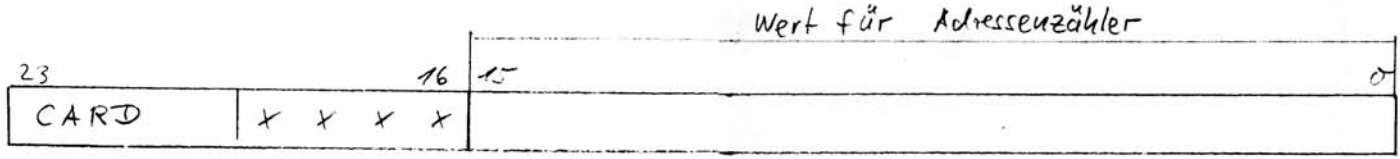
009. A ADDRESS INTERPRETATION

10.10.195 dlu

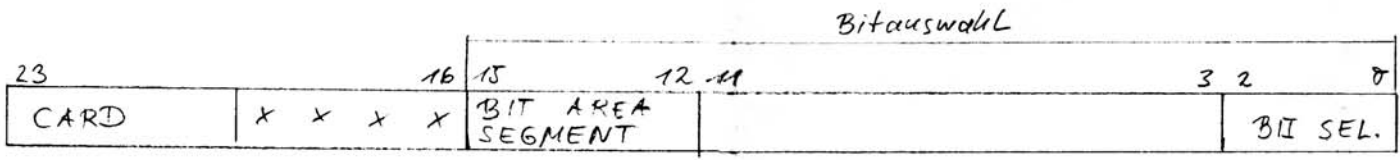
2



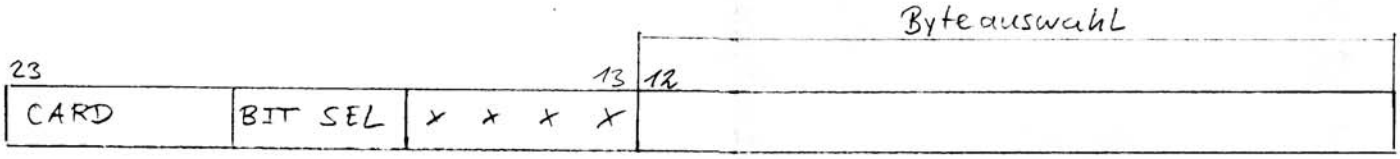
a.) Bytezugriffe zu MMC



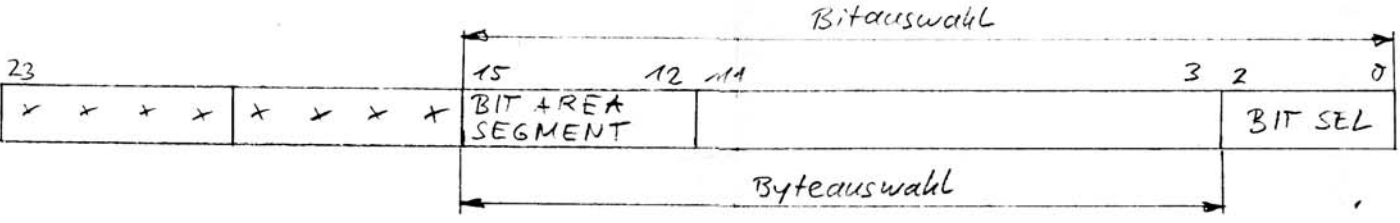
b.) Laden Adressenzähler in MMC



c.) Bitzugriffe (normal) zu BMC

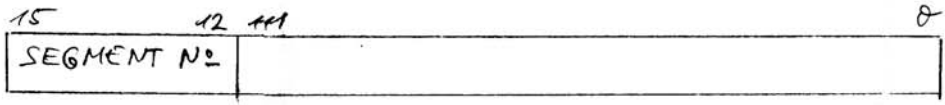


d.) Bitzugriffe (vertikal) zu BMC

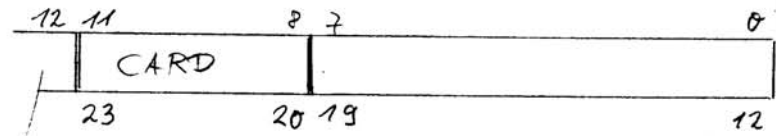


e.) Adresse im COMPARE MODE

Bildung der 24-Bit-Adresse



CPU-Adresse



Wort in Segment-RAM

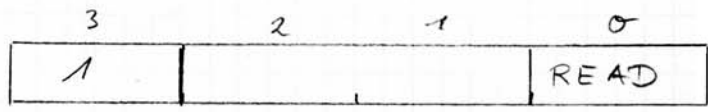
ACCESS CONTROL

009. A MODE INTERPRETATION

10.10.95 (1a)

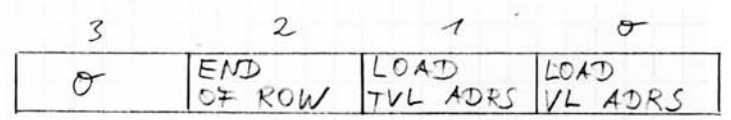
3

a.) ACCESS MODE



MODE	BMC	MMC
8	WRITE BYTE	WRITE BYTE
9	READ BYTE	READ BYTE
A	WRITE BIT	-
B	READ BIT	-
C	WRITE MODE REG	WRITE MODE REG.
D	READ BIT SEGMENT ADRS	READ MATCH
E	WRITE BIT SEGMENT ADRS	WRITE ADRS
F	DO NOTHING	DO NOTHING

b.) COMPARE MODE



MODE REG INTERPRETATION

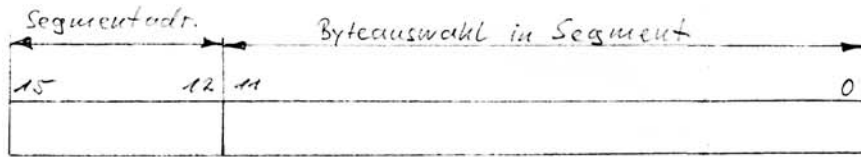
CONTENT	BMC	MMC
4	NORMAL ACCESS	DO NOTHING (NORMAL ACCESS ONLY)
1	VERTICAL BIT ACCESS	VL MEMORY
2	VA MEMORY, BINARY	TVL MEMORY 1)
3	VA MEMORY, TERNARY	TVL MEMORY 2)

1) MATCH ← /MATCH FLIPFLOP

2) MATCH ← MATCH FLIPFLOP

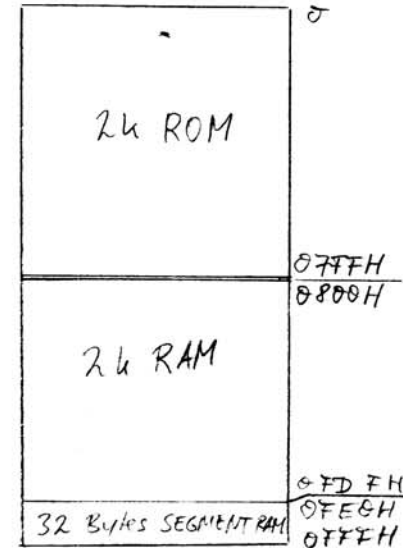
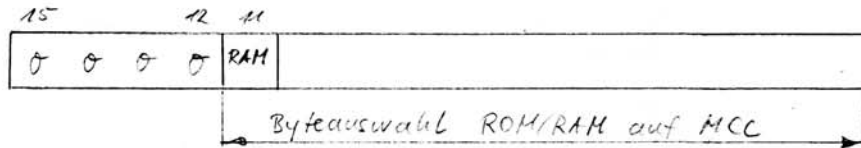
009. A CPU ADRS INTERPRETATION

4

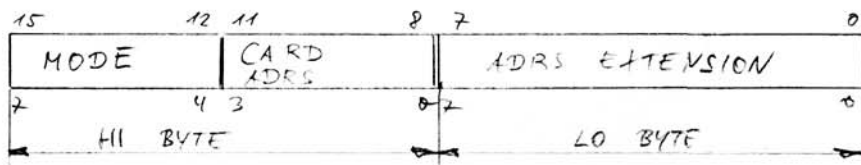


Speicheraufteilung auf MCC

Segment 0 (ROOT SEGMENT)



Inhalt des SEGMENT RAM



MODE FIELD INTERPRETATION

MODE FIELD FOR INTERNAL ACCESS

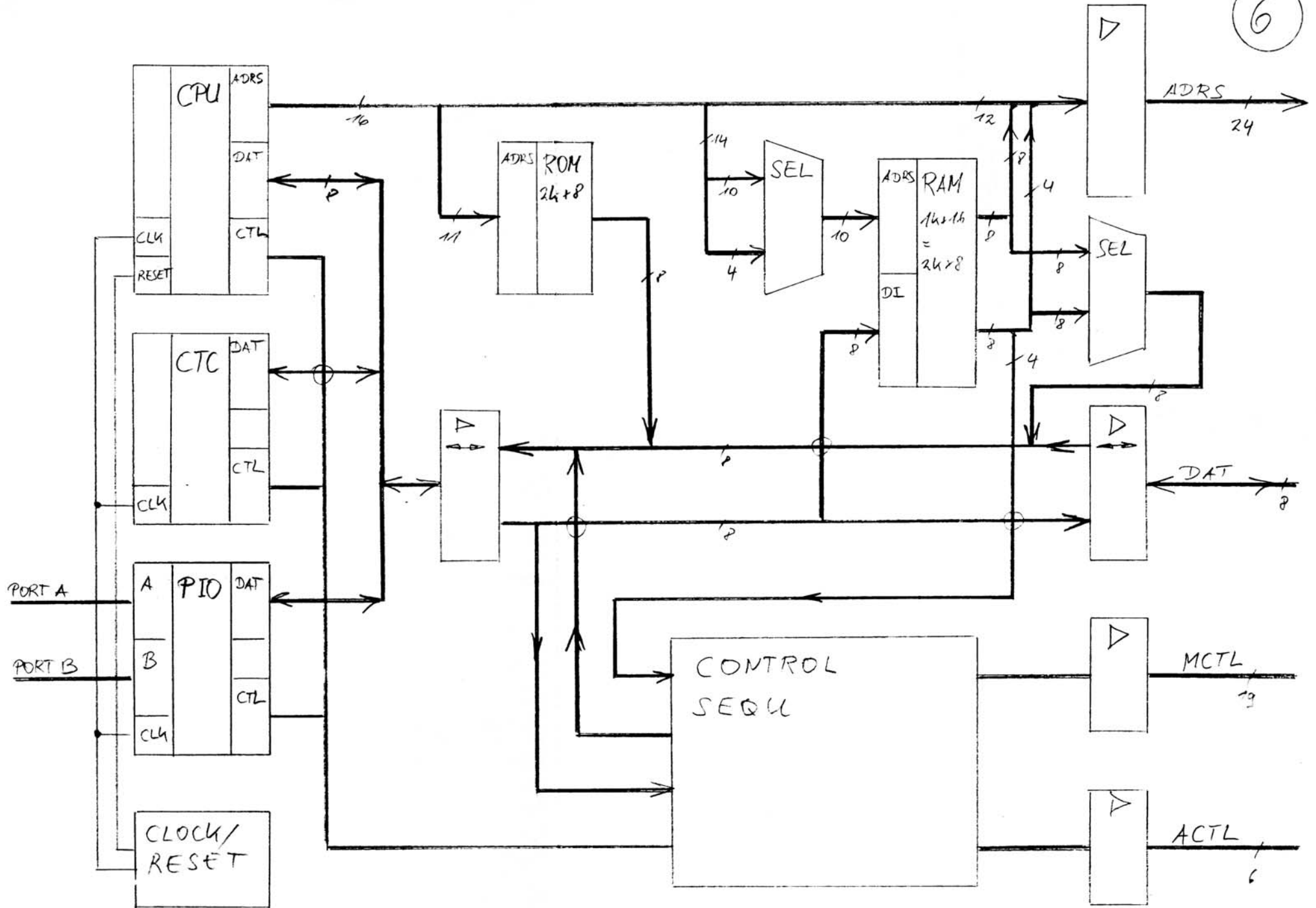
- 9 - LOAD ROW COUNT LO
- A - LOAD ROW COUNT HI
- B - LOAD VAR COUNT LO
- C - LOAD VAR COUNT HI
- D - READ STATUS

CONTENT	BMC	MMC
0	BYTE ACCESS	BYTE ACCESS
1	BIT ACCESS	-
2	MODE REG ACCESS	MODE REG ACCESS
3	BIT SEGMENT ADRS ACCESS	READ MATCH / WRITE ADRS
E	COMPARE	COMPARE
F	DO NOTHING	DO NOTHING

009. A MASTER CONTROL CARD (MCC)

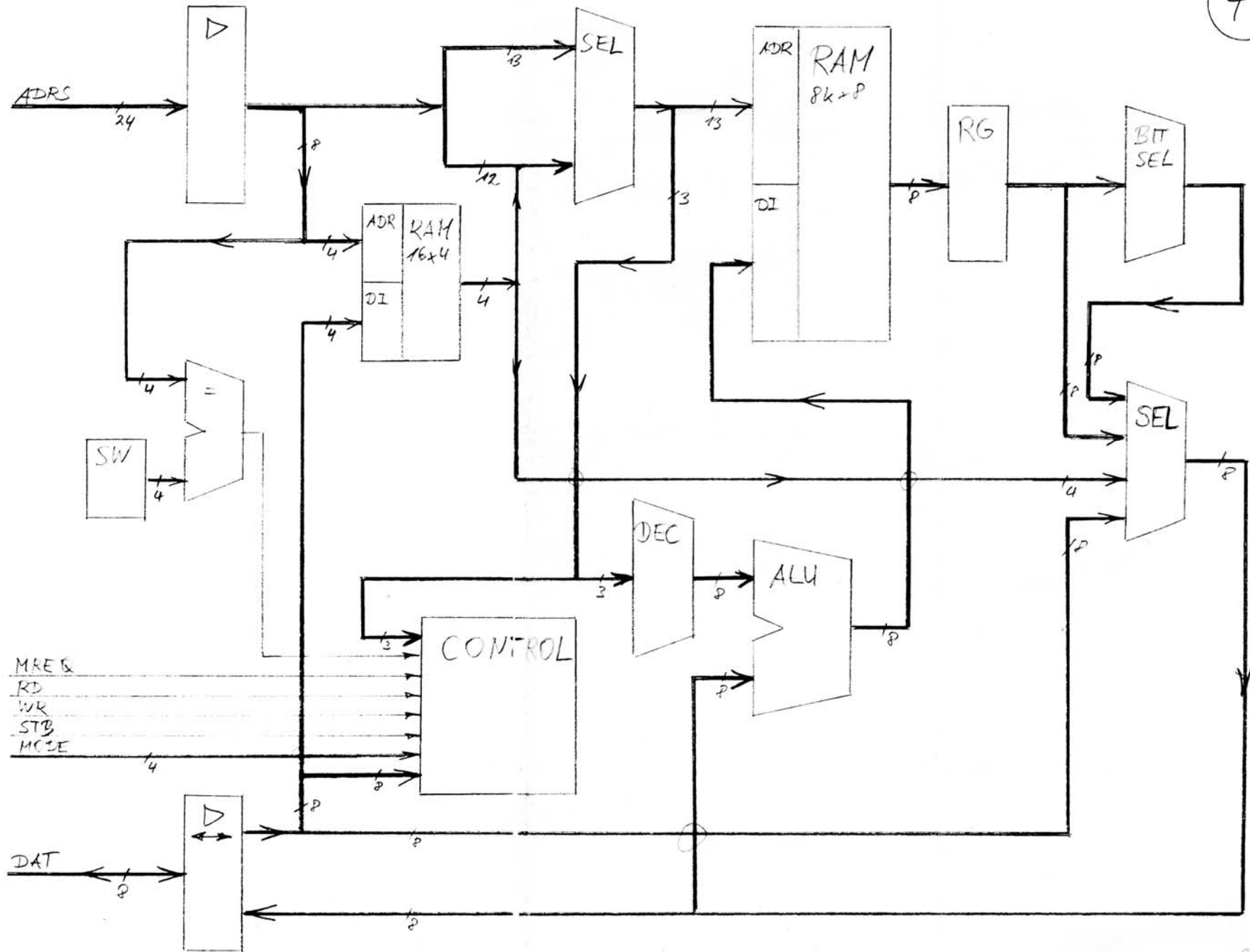
- DATA FLOW OVERVIEW -

6



009. A BIT ACCESS MEMORY CARD (BMC) - DATA FLOW OVERVIEW -

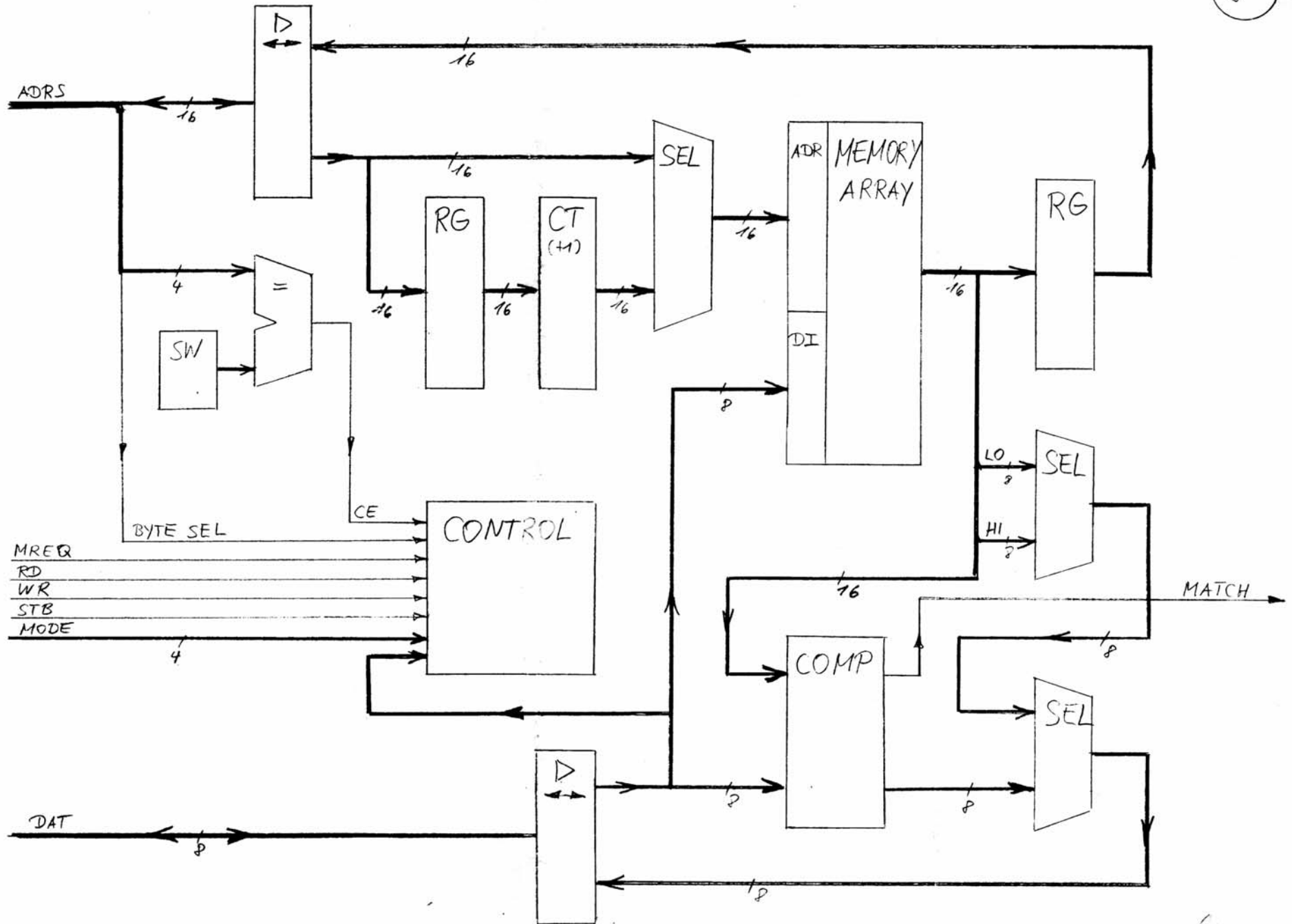
7



10.10.85 lla

009. A MULTIFUNCTION MEMORY CARD (MMC) - DATA FLOW OVERVIEW -

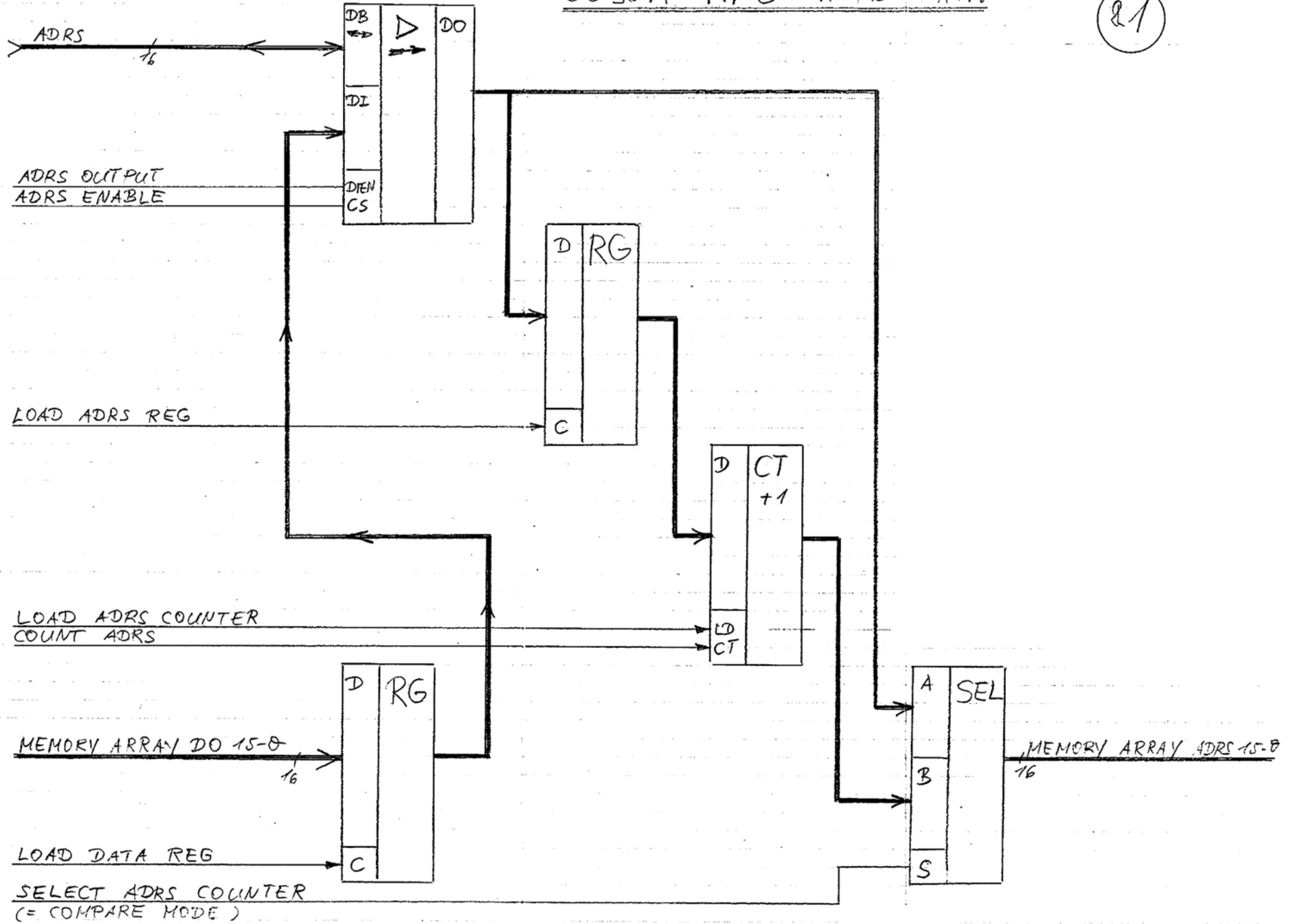
8



10.10.85 [Signature]

009. A MMC ADRS PATH

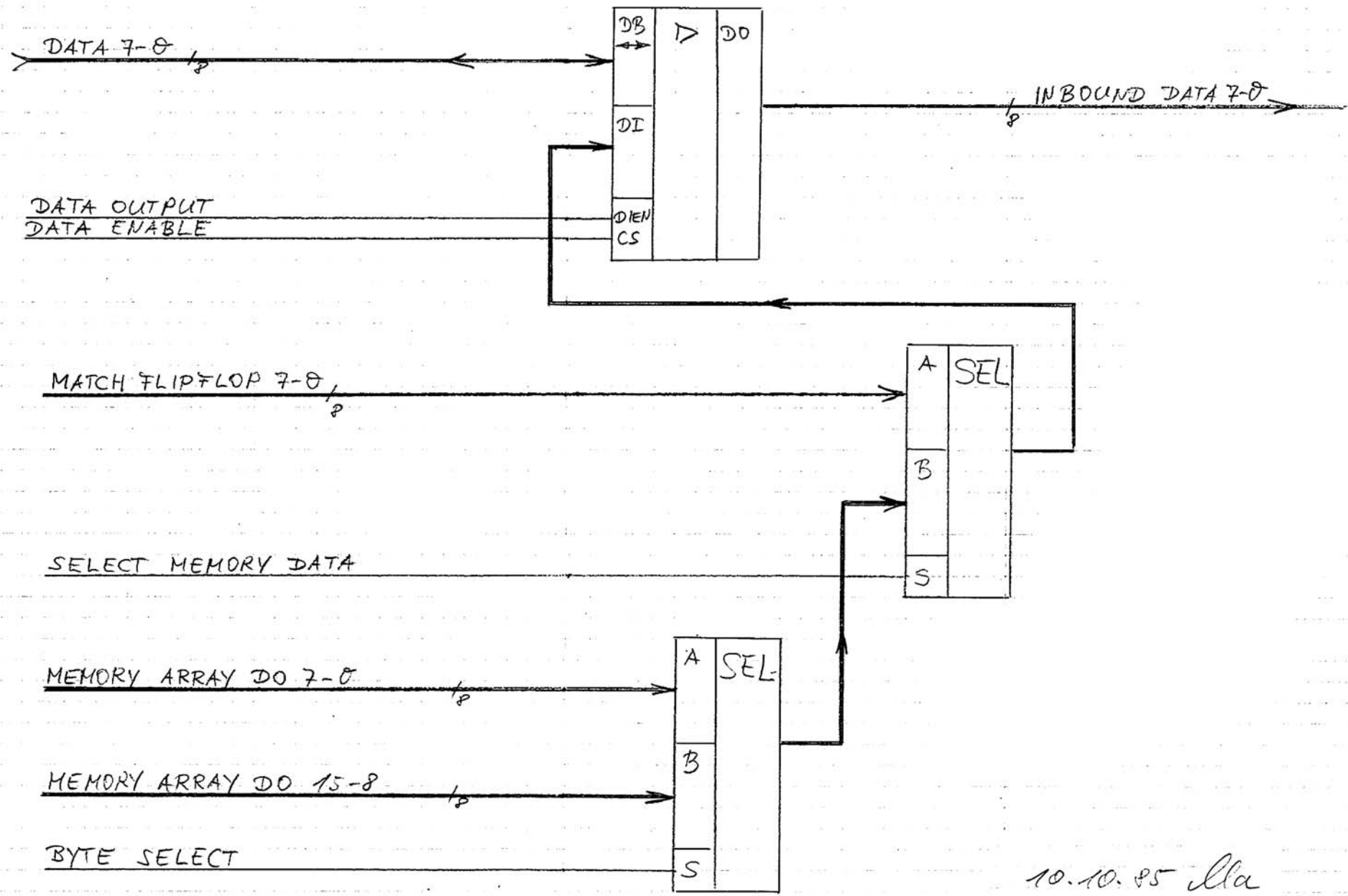
21



10-10-85 *Clax*

009. A MMC DATA PATH

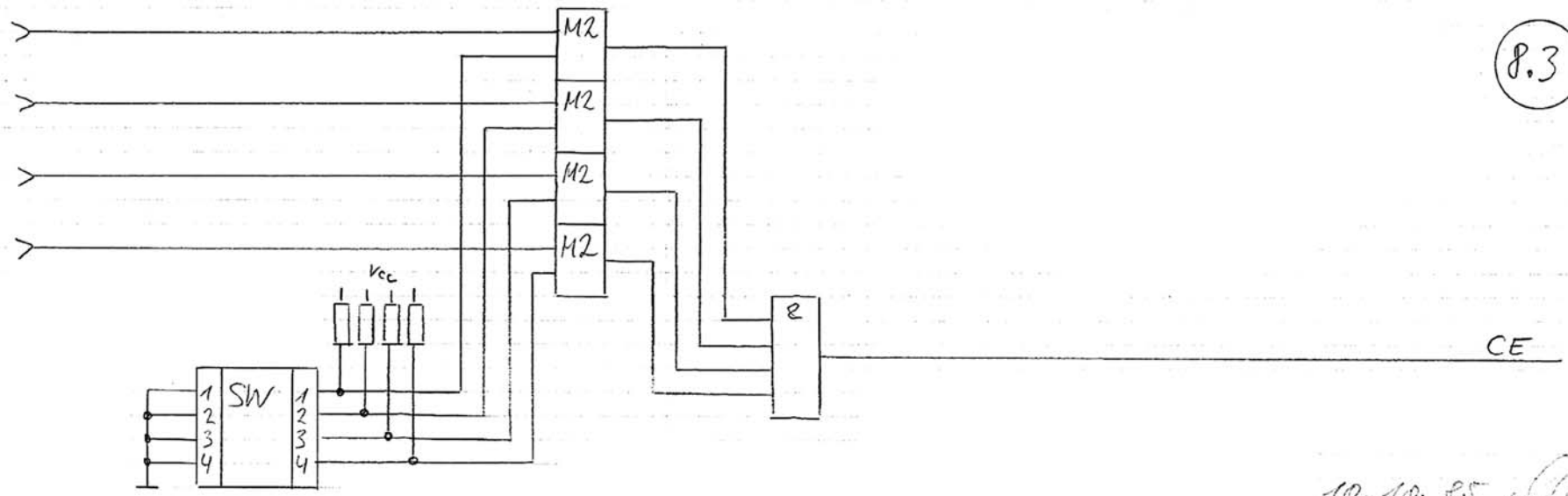
8.2



10.10.95 *lla*

009.A MMC MODULE ADRS DECODE

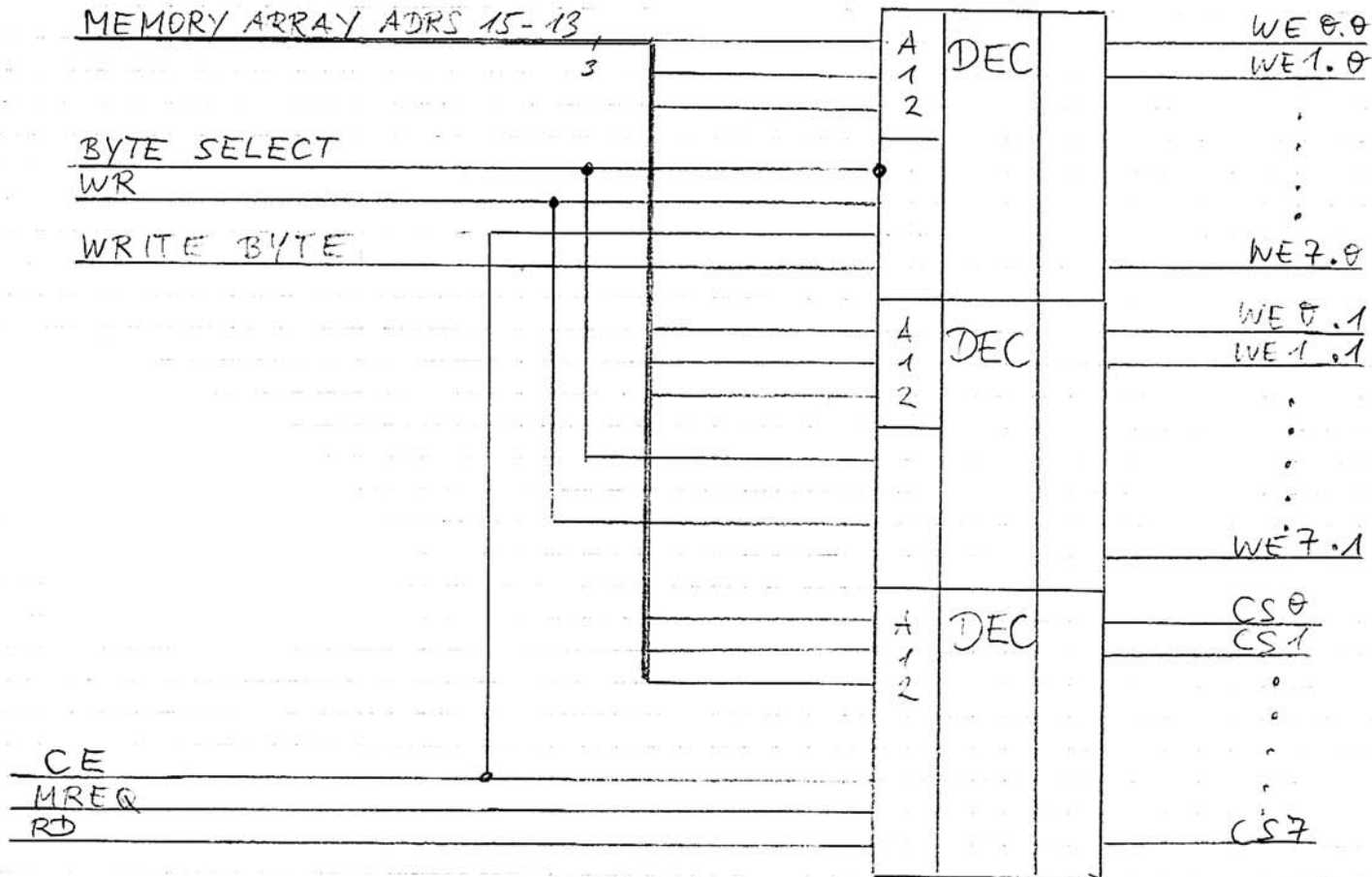
8.3



10-10-95 Jlu

009.A MMC MEMORY ADDR DECODE

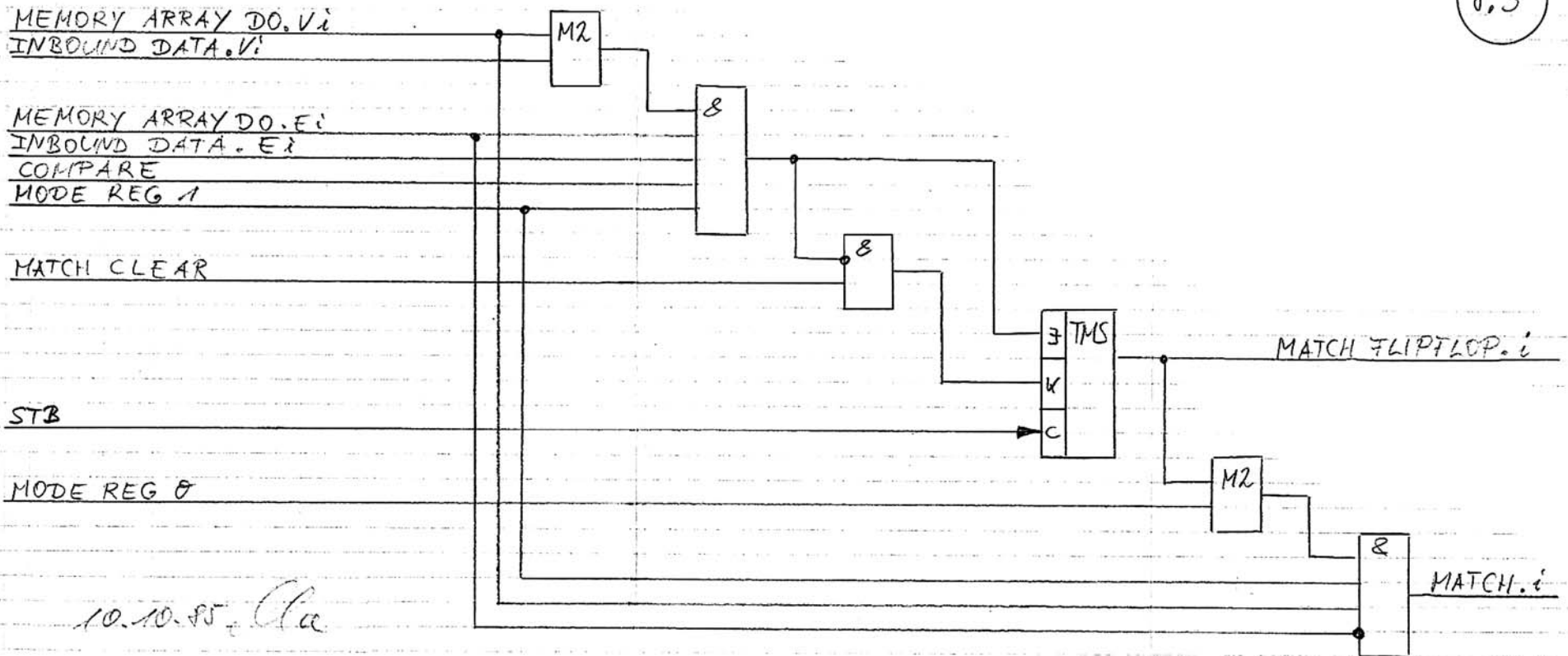
8.4



10-10-85 16:00

009.A MMC COMPARE POSITION

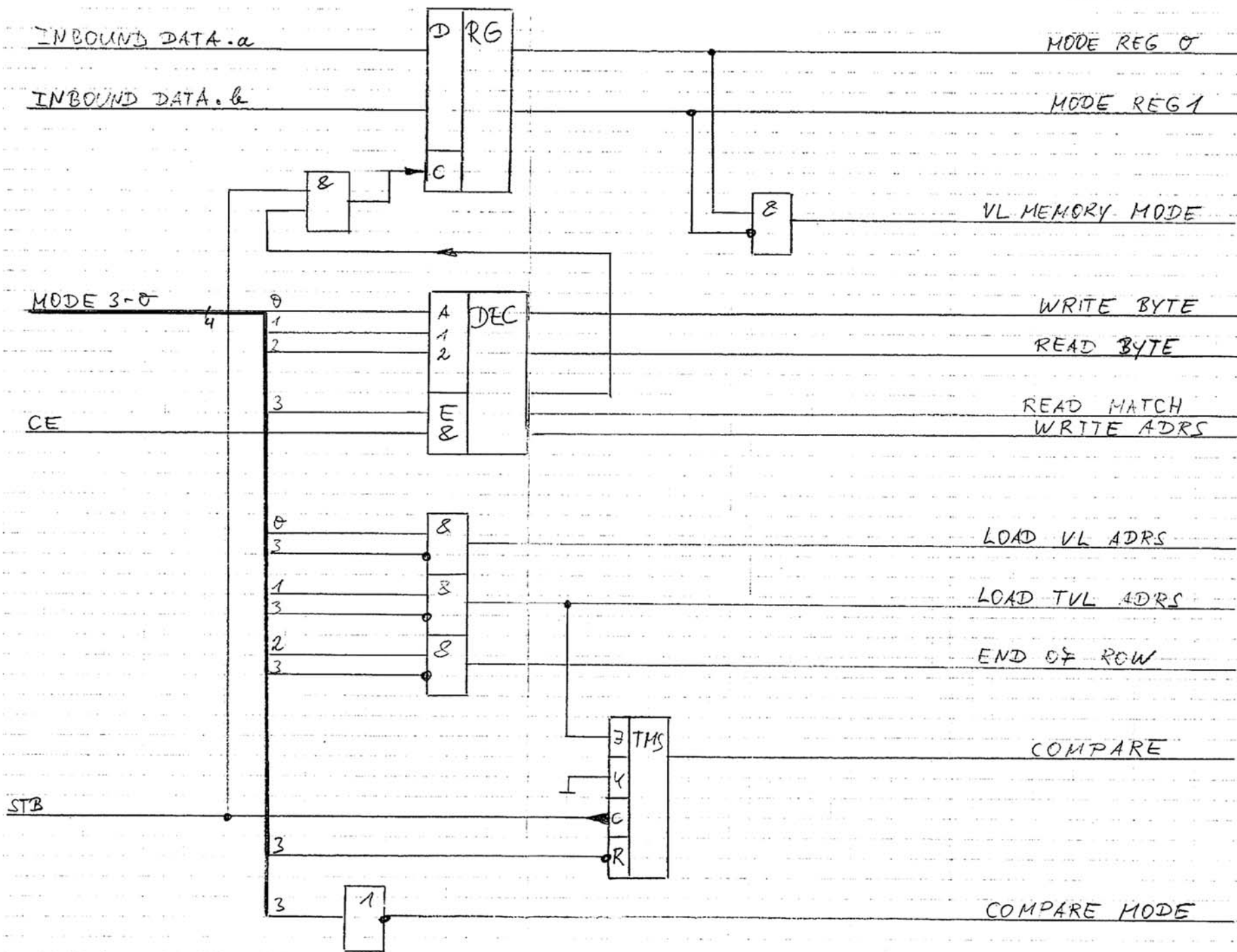
8.5



10.10.85, Acc

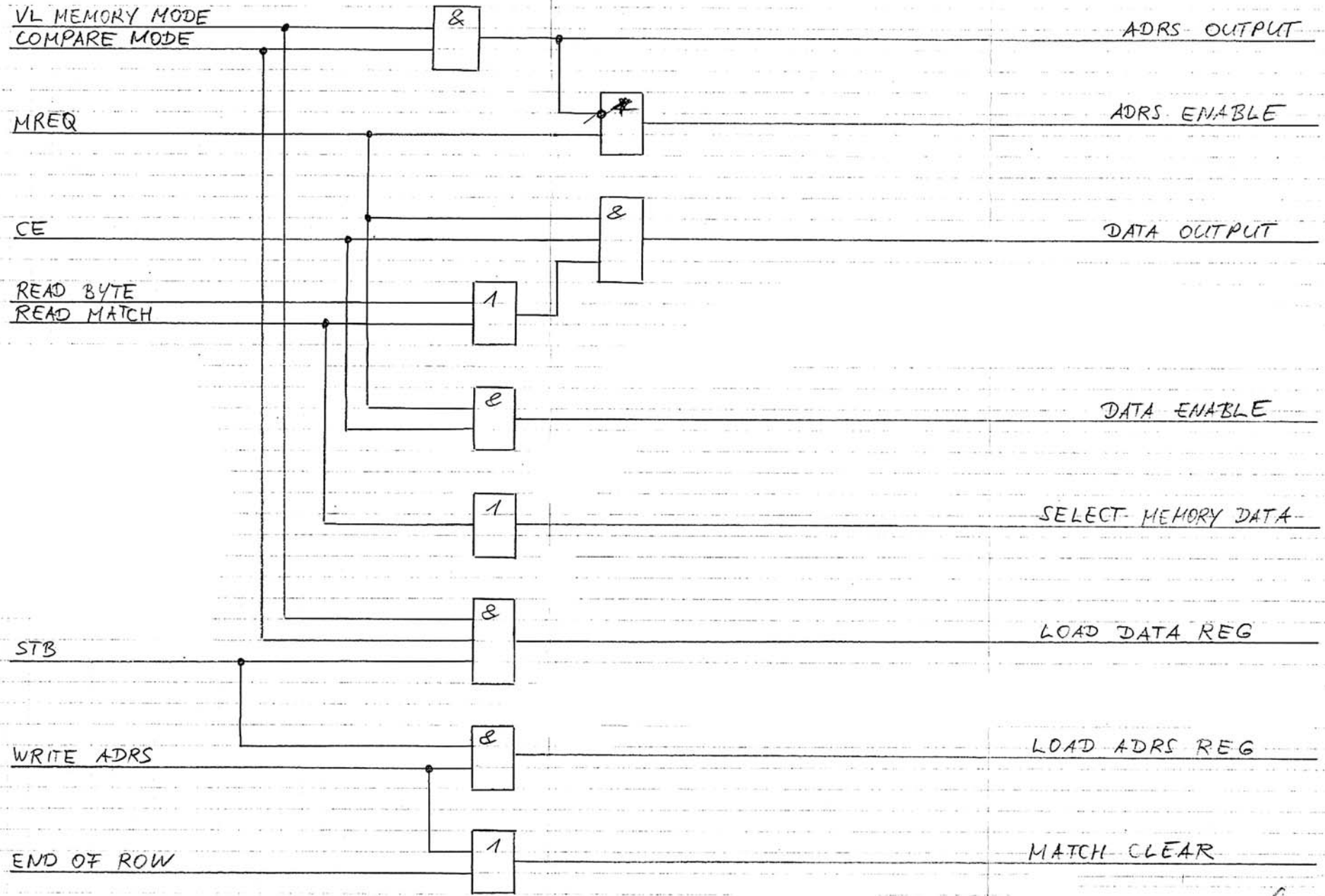
009.A M.M.C CONTROL I

8.6



8.7

009.A MMC CONTROL II



10.10.85 Ma

009.A MMC

MEMORY OPERATION CHIP (MOC)

8.9

ADRS ↔ 0 1 2 3	009.A MOC	MADR 0 1 2 3
DAT ↔ 0 1		
MDO 0 1 2 3		MOI 0 1
MODE 0 1 2 3		
-STB MREQ CARRY IN		MATCH CARRY OUT
BYTE SEL CE		WRITE BYTE

10.10.85 *llc*

ent. node -1 Eingang FIRST POSITION