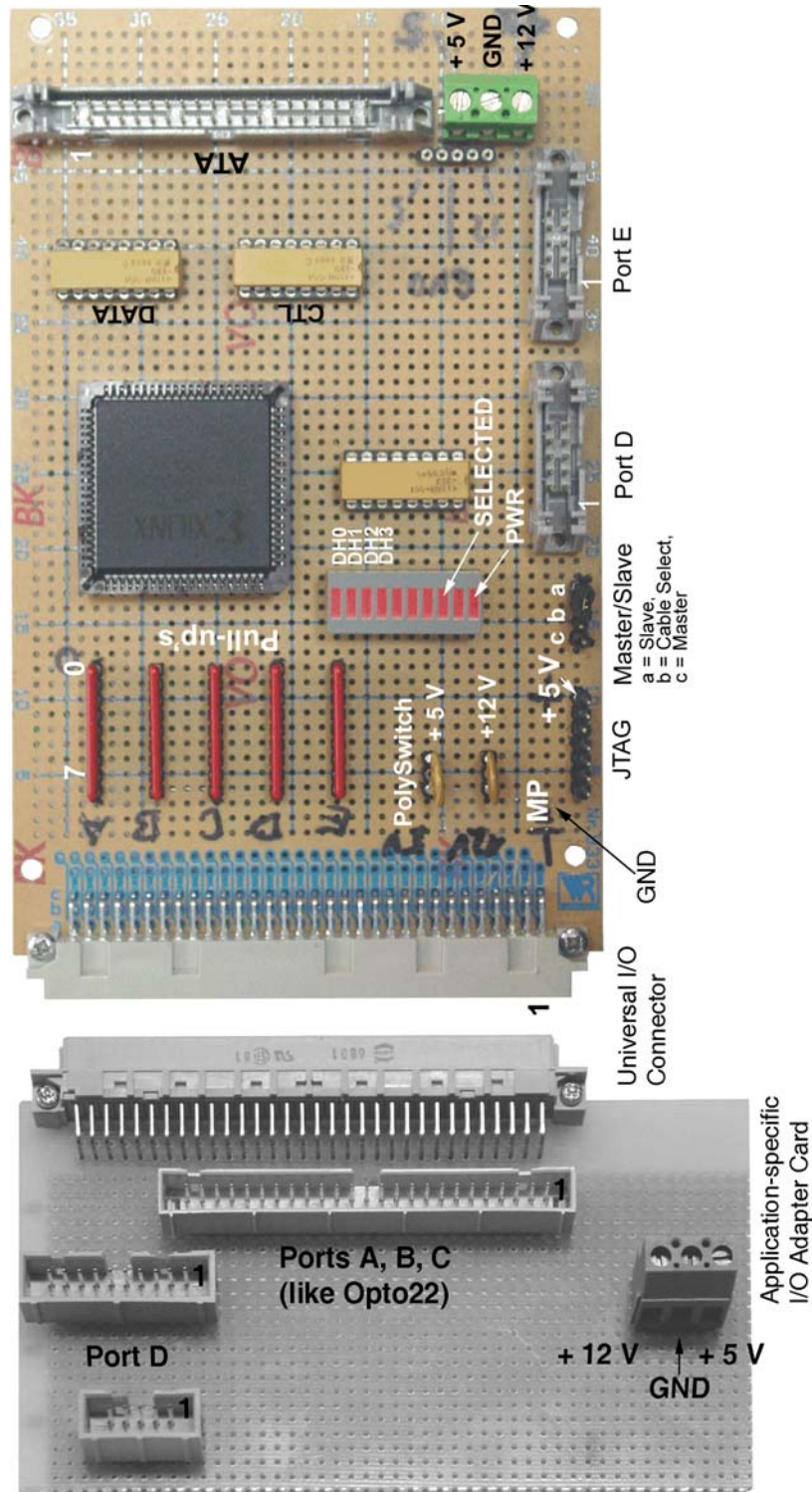


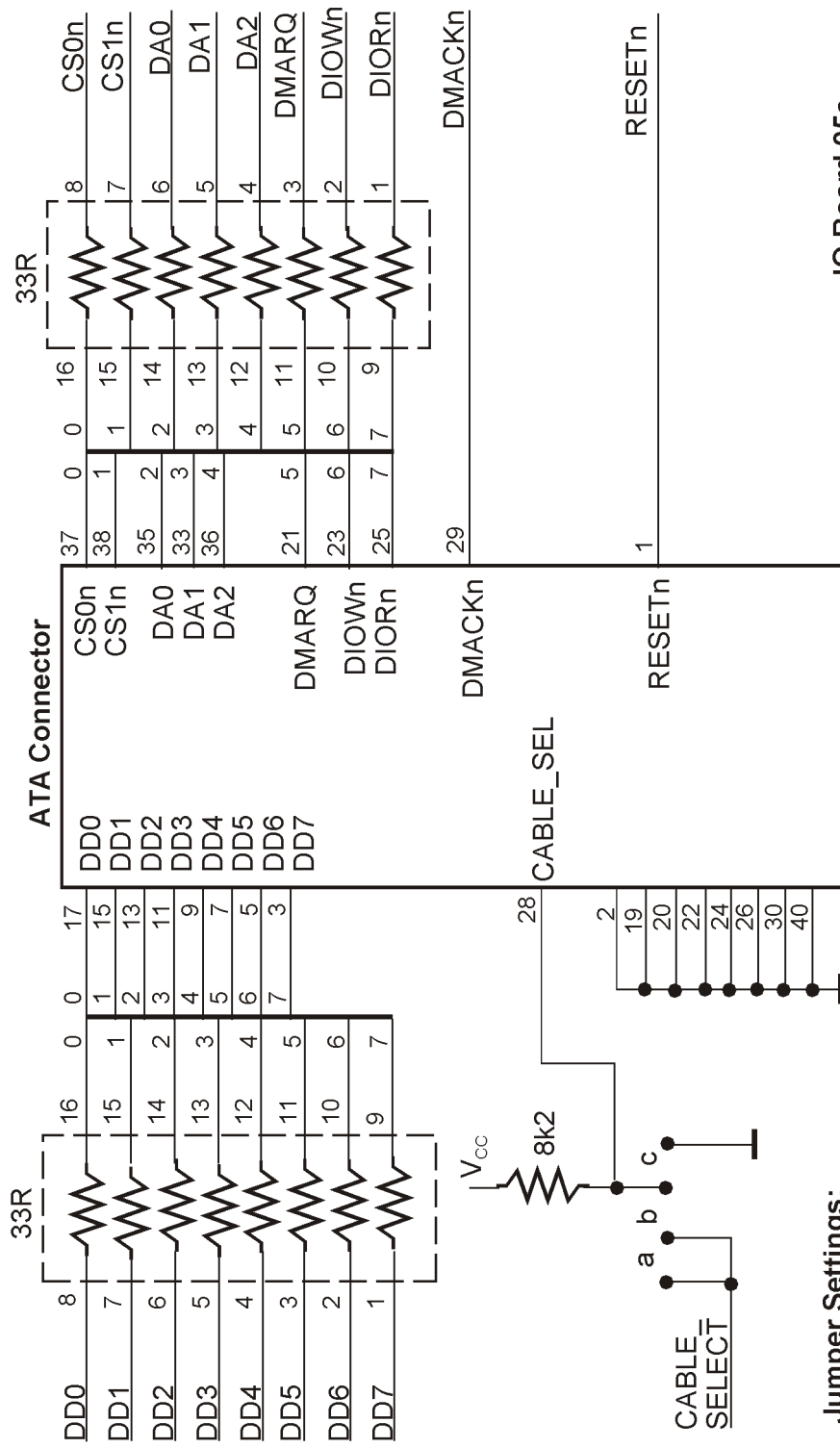
ATA-to-ISA Board 07a

– Schematics –

This experimental board contains an ATA IO port adapter 05a in a Xilinx 95108 CPLD.

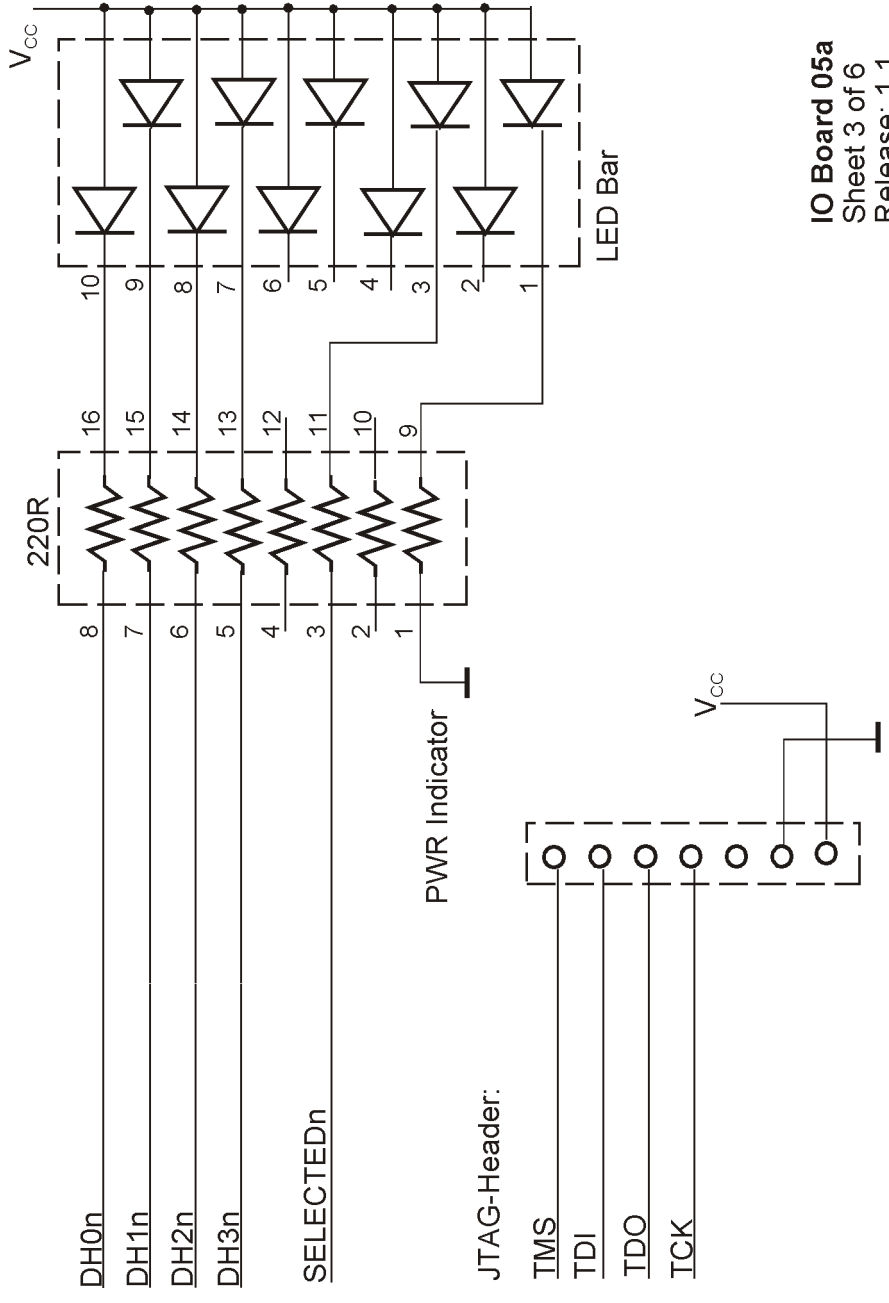
For more details see <http://www.controllersandpcs.de/ataio>.



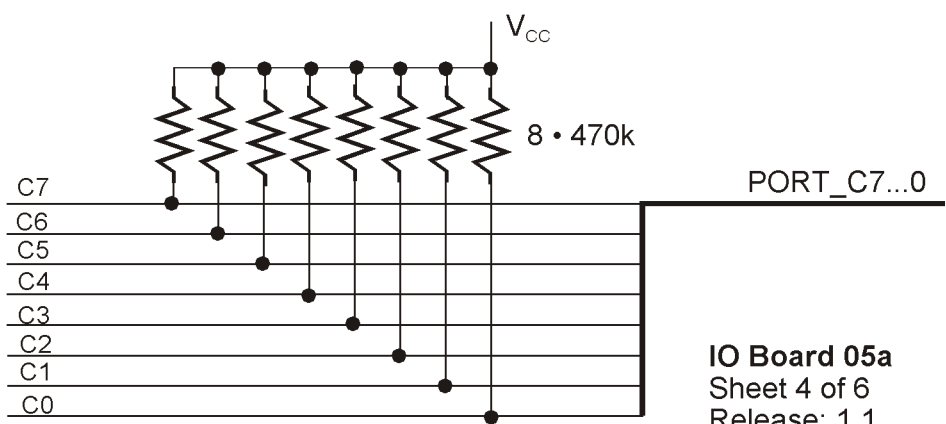
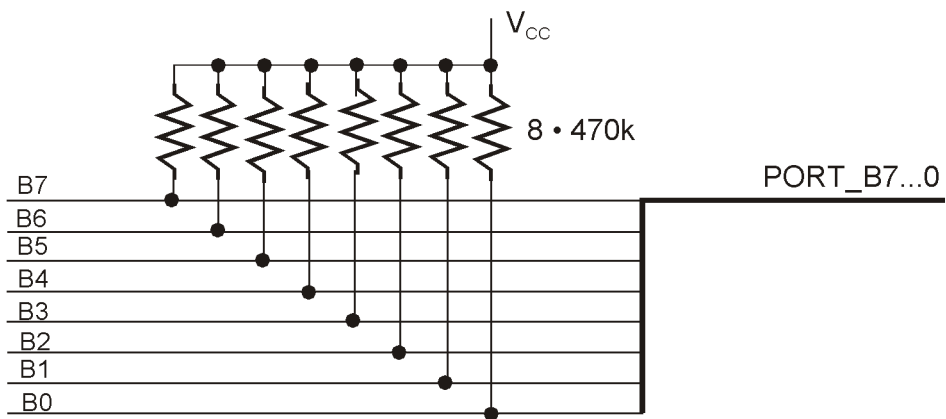
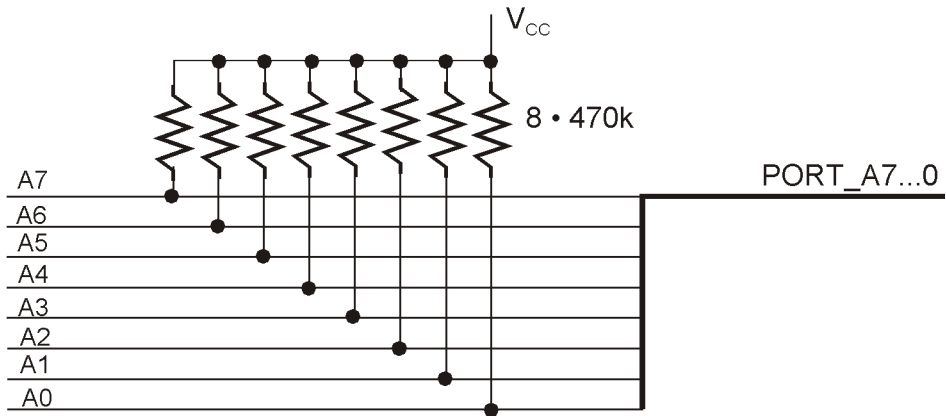


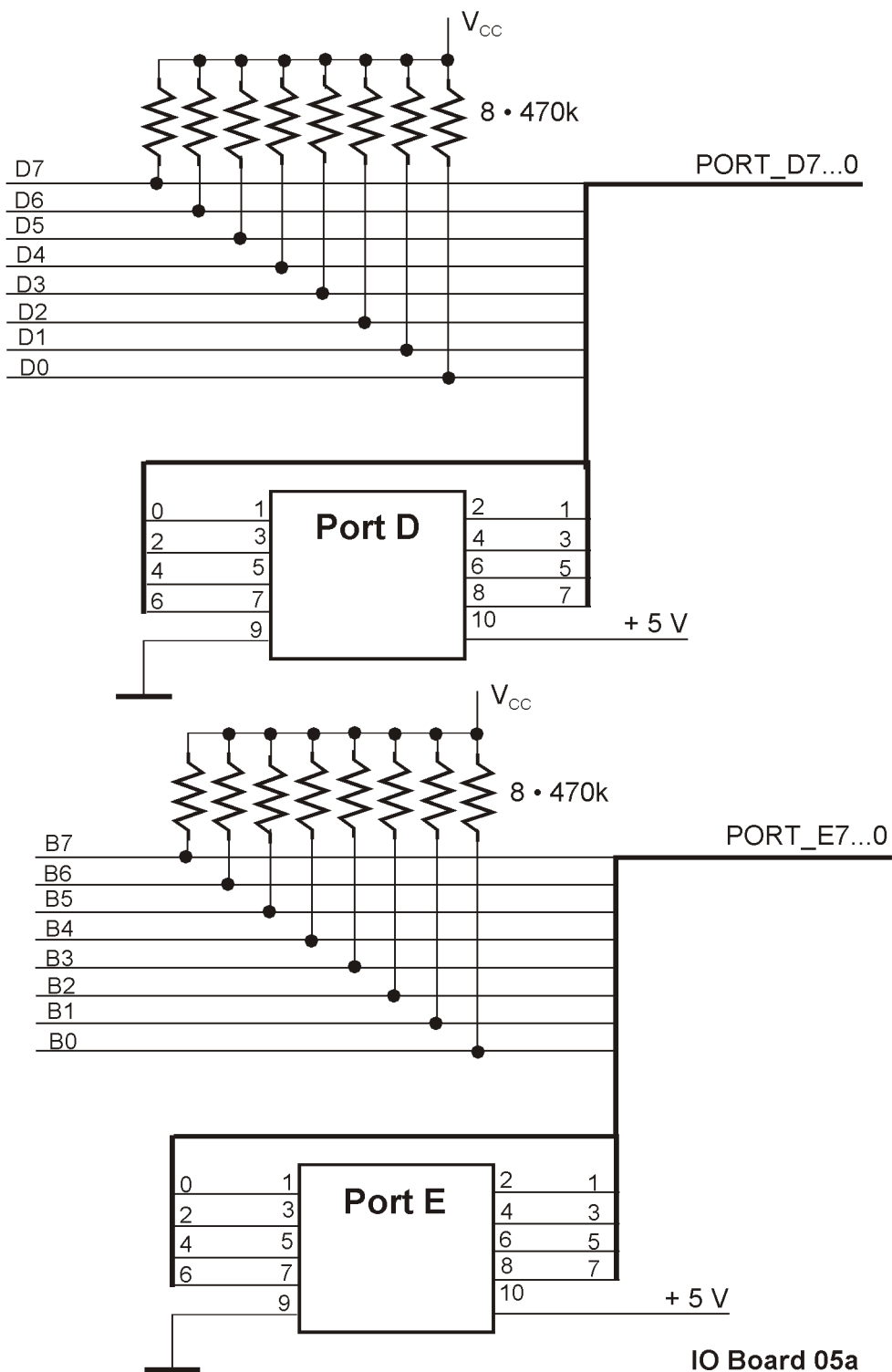
Jumper Settings:
 a – Slave (Jumper in Parking Position)
 b – Cable Select
 c – Master

ATA05a			
51	DD0	A0	5
23	DD1	A1	32
52	DD2	A2	80
67	DD3	A3	33
83	DD4	A4	19
11	DD5	A5	34
40	DD6	A6	63
24	DD7	A7	45
44	DA0	B0	3
70	DA1	B1	4
26	DA2	B2	75
		B3	79
54	CS0n	B4	17
69	CS1n	B5	18
		B6	61
9	DIOR-	B7	62
10	DIOW-		
		C0	7
55	DMARQ	C1	37
56	DMACKn	C2	82
		C3	39
31	CSEL	C4	21
		C5	48
74	RESETn	C6	66
		C7	50
22	V _{CC}	D0	6
38		D1	35
64		D2	81
73		D3	36
78		D4	20
		D5	46
		D6	65
8	GND	D7	47
12		E0	1
16		E1	2
25		E2	71
27		E3	72
42		E4	14
49		E5	15
60		E6	57
77		E7	58
		REO	68
76	REI		
		SELECTEDn	53
		DH0n	13
		DH1n	41
		DH2n	84
		DH3n	43
28	TDI		
29	TMS		
30	TCK	TDO	59



IO Board 05a
 Sheet 3 of 6
 Release: 1.1





DIN 41612
I/O Connector

