ATA I/O Adapter 8255a

Programmer's Reference / Hardware Description

Release: 1.2 vom 19. 9. 06

Purpose:
Attachment of three to five general-purpose I/O ports (8 bits each) to a parallel ATA interface (fig. 1). Three of those ports correspond to the industry standard programmable peripheral interface (PPI) 8255 (mode 0 only).

ATA I/O adapter 8255_01:
Only three 8255- like I/O ports (A, B, C). The 8255 mode register can be read back.

ATA I/O adapter 8255_02:
Five I/O ports (A...E). Ports A, B, C correspond to the 8255 PPI (mode 0). The 8255 mode register is a write-only register. The ports D and E are true general-purpose I/O ports. Under program control, each of the 2 • 8 = 16 I/O lines can be used as an input or as an output.

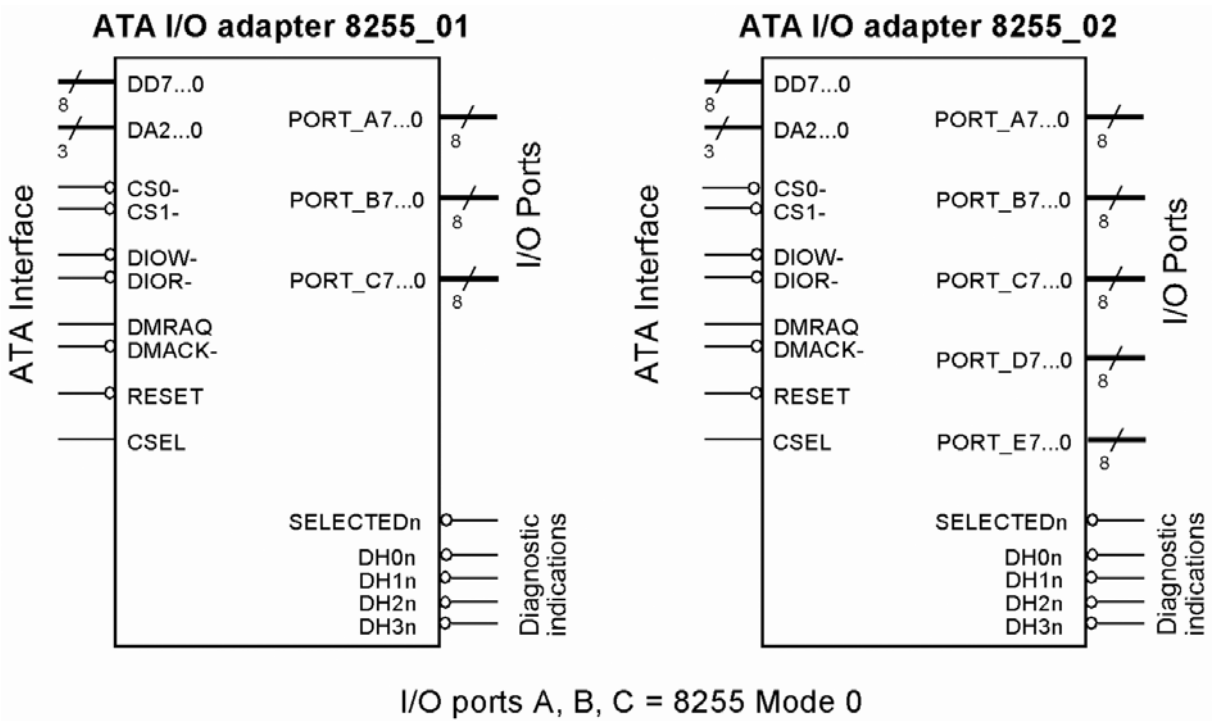


Fig. 1 ATA I/O adapter ICs comprising three or five I/O ports.

ATA signals supported:

- DD7...0 (8 bit data bus)
- CS0, CS1
- DA2, DA1, DA0
- DIOW, DIORD
- DMARQ, DMACK
- RESET
- CSEL

ATA signals not supported:

- DD15...8
- INTRQ, IORDY
- DASP, PDIAG

Principles of I/O port operation (1): Ports A, B, C
Those I/O ports behave like the ports of a compatible to the industry standard programmable peripheral interface (PPI) 8255, operated in mode 0. Each of the ports comprises a data register. All three ports are controlled by a common mode register (fig. 2, table 1). The bit positions 4, 3, 1, 0 control the direction of the corresponding I/O signals:

- If the mode bit is set to zero, the particular I/O port is configured as an output, the port driver being in high impedance state.
- If the mode bit is set to one, the particular I/O port is configured as an intput. The potential (low or high) on the I/O pins correspond to the content of the data register.

After reset:
Mode register positions 4, 3, 1, 0 = 0 (all I/O pins are in high impedance state); all data registers contain 00H.

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	0	0	Port A I/O	Port C_H I/O	0	Port B I/O	Port C_L I/O
	Group A				Group B		

Fig. 2 The 8255-like mode register.

Mode register bit position	**I/O ports controlled**
0	Port C3...0 (low-order nibble)
1	Port B7...0
3	Port C7...4 (high-order nibble)
4	Port A7...0

Table 1 Mode register bit positions and I/O ports.

Principles of I/O port operation (2): Ports D, E
The I/O ports are similar to the typical I/O ports of well-known microcontroller families (Microchip PIC, Atmel AVR and the like). Each I/O port comprises a direction control register (DIR) and a data register (DAT). The DIR bit positions control the direction of the corresponding I/O signals (fig. 3):

- If the DIR bit is set to zero, the corresponding I/O pin is configured as an input, the pin driver being in high impedance state.
- If the DIR bit is set to one, the corresponding I/O pin is configured as an output. The potential (low or high) on the I/O pin corresponds to the bit in the DAT register.

After reset:
DIR = 00H (all I/O pins are in high impedance state), DAT = 00H.

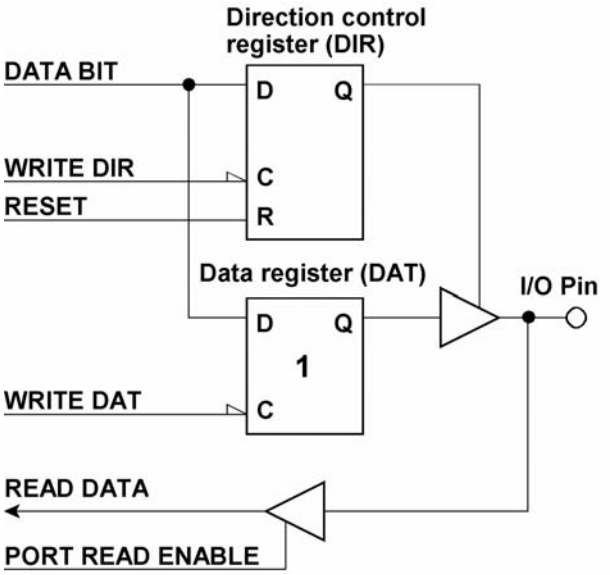


Fig. 3 Principal structure of an I/O bit position.

ATA device selection
Via the CSEL input, the I/O adapter can be configured as device 0 (master) or device 1 (slave):

- CSEL = 0: Master (Device 0),
- CSEL = 1: Slave (Devicve 1).

Typically, CSEL will be wired to Low or High potential or connected to the CSEL line of the ATA interface (Cable Select).

I/O addressing
Three port addresses in the DH register are assigned to the ATA I/O adapter (fig. 4, tables 2 to 4). The 8255 ports have one common port address. The general-purpose ports have separate port addresses.

7	6	5	4	3	2	1	0
-	-	-	DEVICE	I/O Port Selection (Port Address)			

Fig. 4 DH register content.

DH register bits 3... 0	I/O port
6H	Ports A, B, C
7H	Port D*)
8H	Port E*)
all other values	no effect

*): 8255_02 only.

Table 2 I/O Port addressing via DH register.

I/O port selection
Writing into a register of or reading from an I/O port requires two steps:

1. Select the ATA device and the I/O port by writing into the DH register.

2. Write to or read from either the particular register of the selected port.

A port address loaded into the DH register will be retained. Therefore, if an already selected port is to be accessed, step 1 could be skipped.

CS		Register Address DA				Register	Legacy ATA Ports			
1-	0-	2	1	0	Hex		1	2	3	4
1	0	0	1	0	2	Port A	1F2	172	1EA	0,17
1	0	0	1	1	3	Port B	1F3	173	1EB	16B
1	0	1	0	0	4	Port C	1F4	174	1EC	16C
1	0	1	0	1	5	Mode register	1F5	175	1ED	16D
1	0	1	1	0	6	Device selection and port address register (DH)	1F6	176	1EE	16

Table 3 Register addressing within the 8255 ports A, B, C. Read accesses to one of the ports A, B, C will read back the potentials on the I/O pins.

CS		Register Address DA				Register	Legacy ATA Ports			
1-	0-	2	1	0	Hex		1	2	3	4
1	0	1	0	0	4	Data register (DAT)	1F4	174	1EC	16C
1	0	1	0	1	5	Direction control register (DIR)	1F5	175	1ED	16D
1	0	1	1	0	6	Device selection and port address register (DH)	1F6	176	1EE	16

Table 4 Register addressing within a selected general-purpose I/O port D or E (ATA I/O adapter 8255_02 only). Read accesses to either DAT or DIR addresses will read back the potentials on the I/O pins.

Write operations
A write access to one of the ATA port addresses according to table 2 will write the data byte into the DH register or into a particular register of the selected I/O port (see table 3 or 4). A write access with any other address has no effect upon the I/O adapter.

Writing to the mode register
A write access will be executed only if the bit positions 7, 6, 5, 2 in the data byte correspond to the values shown in fig. 2 (1, 0, 0, 0). The mode cannot be changed. The 8255 bit set / reset format is not supported.

Read operations (1): Ports A, B, C
A read access to one of the port registers A, B, C (see table 3) will return the potentials on the corresponding I/O pins.

The result of a read access to the mode register depends on the adapter type:

- ATA I/O adapter 8255_01: The read access will deliver the contents of 8255 mode register.
- ATA I/O adapter 8255_02: The result of a read acces is not defined.

Read operations (2): Ports D, E
Contrary to the operation of some microcontroller ports (like those of the Atmel AVR controllers), only the potentials (low or high) on the I/O pins can be read back. A read access to the direction control register or to the data register will return the potentials on the corresponding I/O pins.

Read operations (3): Other addresses
If a read access is directed to the DH register or to a port address which does not belong to the allocated range of addresses (selective addressing), the adapter will not act upon the data bus. Thus, the ATA host adapter will deliver a value FFH. The result of read operations with other addresses is not defined.

Selective addressing
Selective addressing is a provision to permit attaching more than one ATA I/O adapter at one interface cable. With this feature implemented, the adapter will only react on the particular port addresses shown in table 2.

Notes:

1. The selective addressing feature can be omitted if the adapter will be the only ATA I/O circuit at the interface cable.

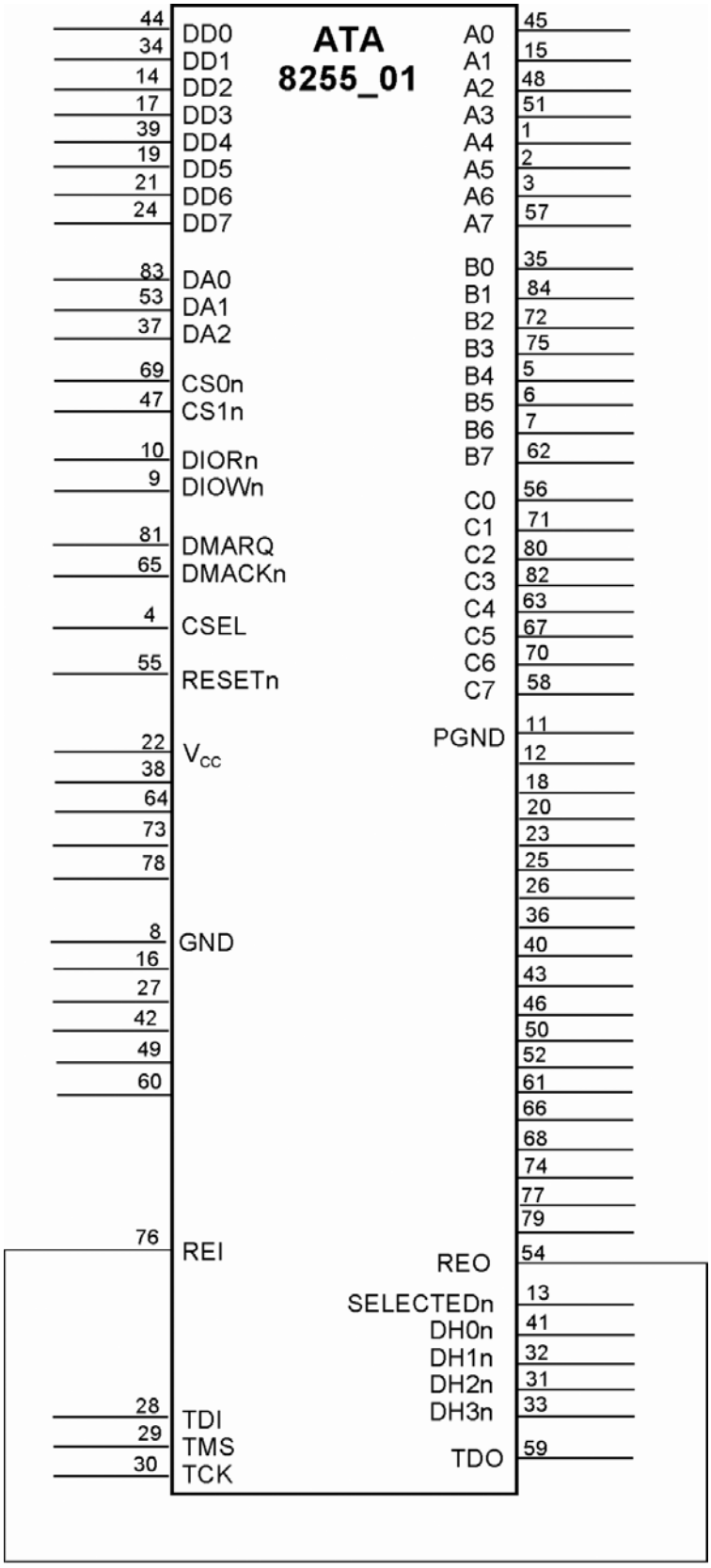
2. If selective addressing is not to be implemented at all, the READ_ADRS input of the ATA I/O front end is to be connected to High potential.

Diagnostic indications:
These signals are provided to drive LEDs (active low). The LEDs will show:

- Whether the adapter has been selected.
- The port address field of the DH Register (DH3...0).

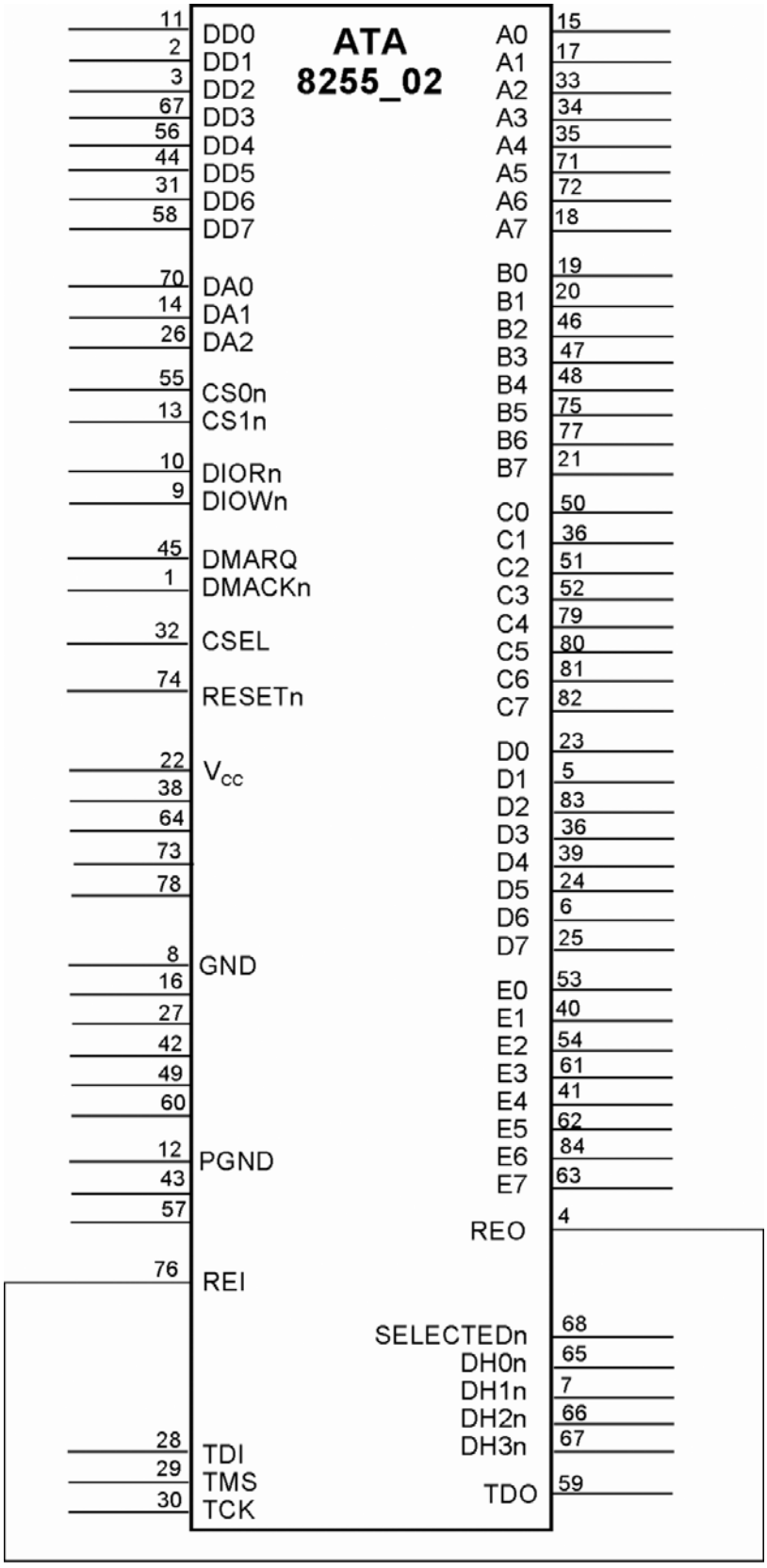
ATA I/O adapter 8255_01 pinout:

Pin No.	Signal Name	Pin No.	Signal Name
1	PORTA<4>	43	PGND
2	PORTA<5>	44	DD<0>
3	PORTA<6>	45	PORTA<0>
4	CSEL	46	PGND
5	PORTB<4>	47	CS1n
6	PORTB<5>	48	PORTA<2>
7	PORTB<6>	49	GND
8	GND	50	PGND
9	DIOWn	51	PORTA<3>
10	DIORn	52	PGND
11	PGND	53	DA1
12	PGND	54	REO
13	SELECTEDn	55	RESETn
14	DD<2>	56	PORTC<0>
15	PORTA<1>	57	PORTA<7>
16	GND	58	PORTC<7>
17	DD<3>	59	TDO
18	PGND	60	GND
19	DD<5>	61	PGND
20	PGND	62	PORTB<7>
21	DD<6>	63	PORTC<4>
22	VCC	64	VCC
23	PGND	65	DMACKn
24	DD<7>	66	PGND
25	PGND	67	PORTC<5>
26	PGND	68	PGND
27	GND	69	CS0n
28	TDI	70	PORTC<6>
29	TMS	71	PORTC<1>
30	TCK	72	PORTB<2>
31	DH2n	73	VCC
32	DH1n	74	PGND
33	DH3n	75	PORTB<3>
34	DD<1>	76	REI
35	PORTB<0>	77	PGND
36	PGND	78	VCC
37	DA2	79	PGND
38	VCC	80	PORTC<2>
39	DD<4>	81	DMARQ
40	PGND	82	PORTC<3>
41	DH0n	83	DA0
42	GND	84	PORTB<1>

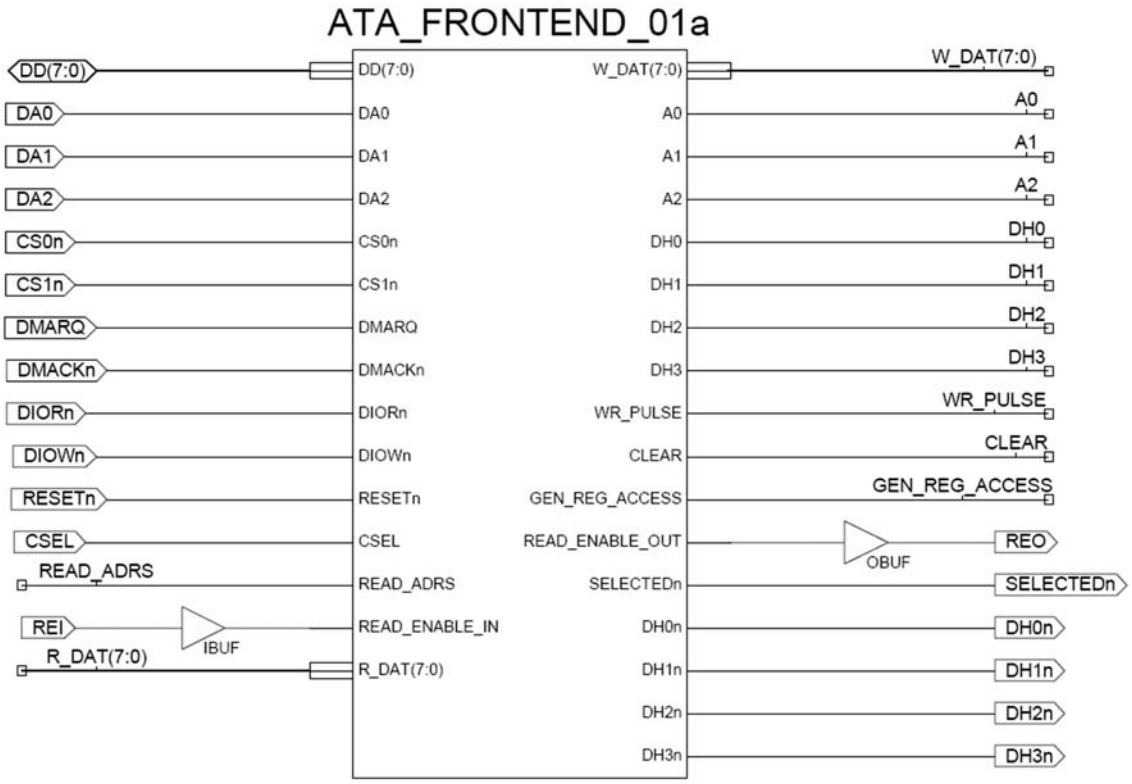

ATA
8255_01
44 DD0
34 DD1
14 DD2
17 DD3
39 DD4
19 DD5
21 DD6
24 DD7
83 DA0
53 DA1
37 DA2
69 CS0n
47 CS1n
10 DIORn
9 DIOWn
81 DMARQ
65 DMACKn
4 CSEL
55 RESETn
22 Vcc
38
64
73
78
8 GND
16
27
42
49
60
76 REI
28 TDI
29 TMS
30 TCK
A0 45
A1 15
A2 48
A3 51
A4 1
A5 2
A6 3
A7 57
B0 35
B1 84
B2 72
B3 75
B4 5
B5 6
B6 7
B7 62
C0 56
C1 71
C2 80
C3 82
C4 63
C5 67
C6 70
C7 58
PGND 11
12
18
20
23
25
26
36
40
43
46
50
52
61
66
68
74
77
79
REO 54
SELECTEDn 13
DH0n 41
DH1n 32
DH2n 31
DH3n 33
TDO 59

ATA I/O adapter 8255_02 pinout:

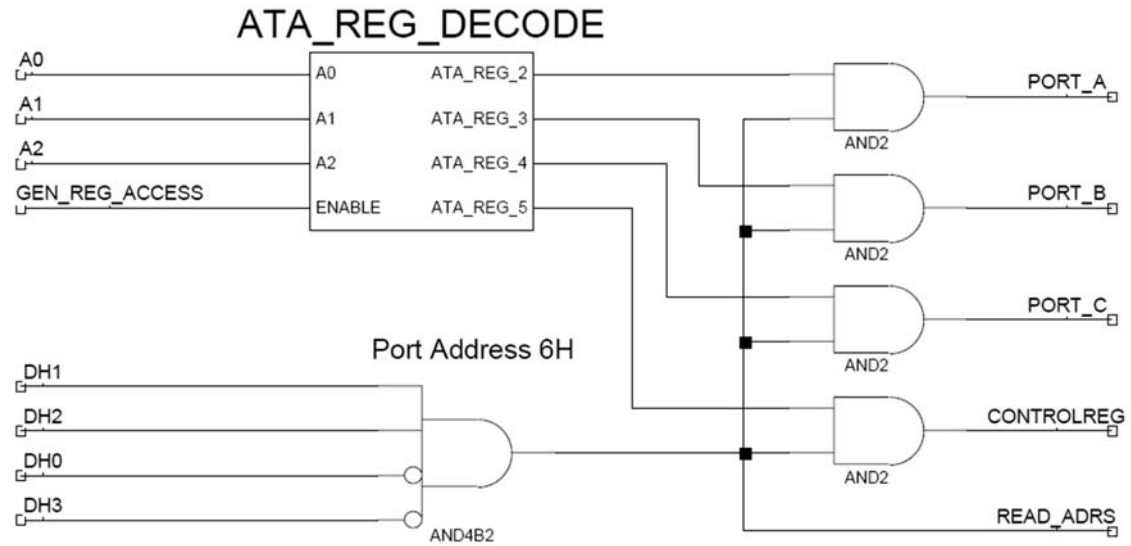
Pin No.	Signal Name	Pin No.	Signal Name
1	DMACKn	43	PGND
2	DD<1>	44	DD<5>
3	DD<2>	45	DMARQ
4	REO	46	PORTB<2>
5	PORTD<1>	47	PORTB<3>
6	PORTD<6>	48	PORTB<4>
7	DH1n	49	GND
8	GND	50	PORTC<0>
9	DIOWn	51	PORTC<2>
10	DIORn	52	PORTD<3>
11	DD<0>	53	PORTE<0>
12	PGND	54	PORTE<2>
13	CS1n	55	CS0n
14	DA1	56	DD<4>
15	PORTA<0>	57	PGND
16	GND	58	DD<7>
17	PORTA<1>	59	TDO
18	PORTA<7>	60	GND
19	PORTB<0>	61	PORTE<3>
20	PORTB<1>	62	PORTE<5>
21	PORTB<7>	63	PORTE<7>
22	VCC	64	VCC
23	PORTD<0>	65	DH0n
24	PORTD<5>	66	DH2n
25	PORTD<7>	67	DH3n
26	DA2	68	SELECTEDn
27	GND	69	DD<3>
28	TDI	70	DA0
29	TMS	71	PORTA<5>
30	TCK	72	PORTA<6>
31	DD<6>	73	VCC
32	CSEL	74	RESETn
33	PORTA<2>	75	PORTB<5>
34	PORTA<3>	76	REI
35	PORTA<4>	77	PORTB<6>
36	PORTC<1>	78	VCC
37	PORTC<3>	79	PORTC<4>
38	VCC	80	PORTC<5>
39	PORTD<4>	81	PORTC<6>
40	PORTE<1>	82	PORTC<7>
41	PORTE<4>	83	PORTD<2>
42	GND	84	PORTE<6>


ATA
8255_02
11 DD0
2 DD1
3 DD2
67 DD3
56 DD4
44 DD5
31 DD6
58 DD7
70 DA0
14 DA1
26 DA2
55 CS0n
13 CS1n
10 DIORn
9 DIOWn
45 DMARQ
1 DMACKn
32 CSEL
74 RESETn
22 Vcc
38
64
73
78
8 GND
16
27
42
49
60
12 PGND
43
57
76 REI
28 TDI
29 TMS
30 TCK
A0 15
A1 17
A2 33
A3 34
A4 35
A5 71
A6 72
A7 18
B0 19
B1 20
B2 46
B3 47
B4 48
B5 75
B6 77
B7 21
C0 50
C1 36
C2 51
C3 52
C4 79
C5 80
C6 81
C7 82
D0 23
D1 5
D2 83
D3 36
D4 39
D5 24
D6 6
D7 25
E0 53
E1 40
E2 54
E3 61
E4 41
E5 62
E6 84
E7 63
REO 4
SELECTEDn 68
DH0n 65
DH1n 7
DH2n 66
DH3n 67
TDO 59

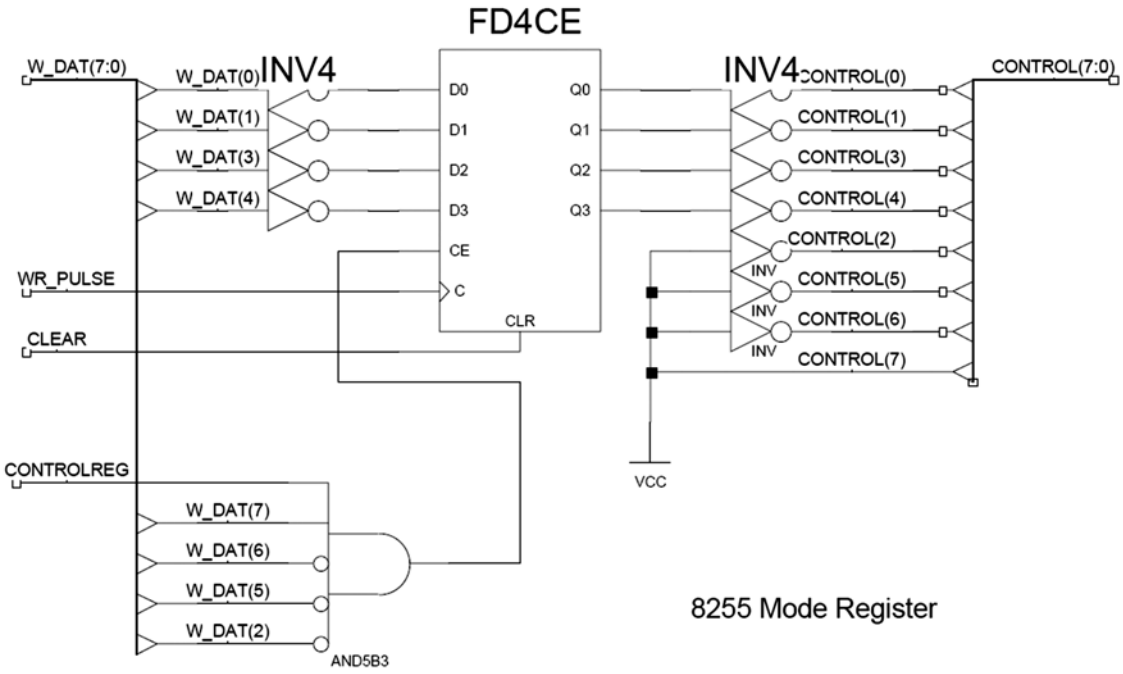
The ATA interface:



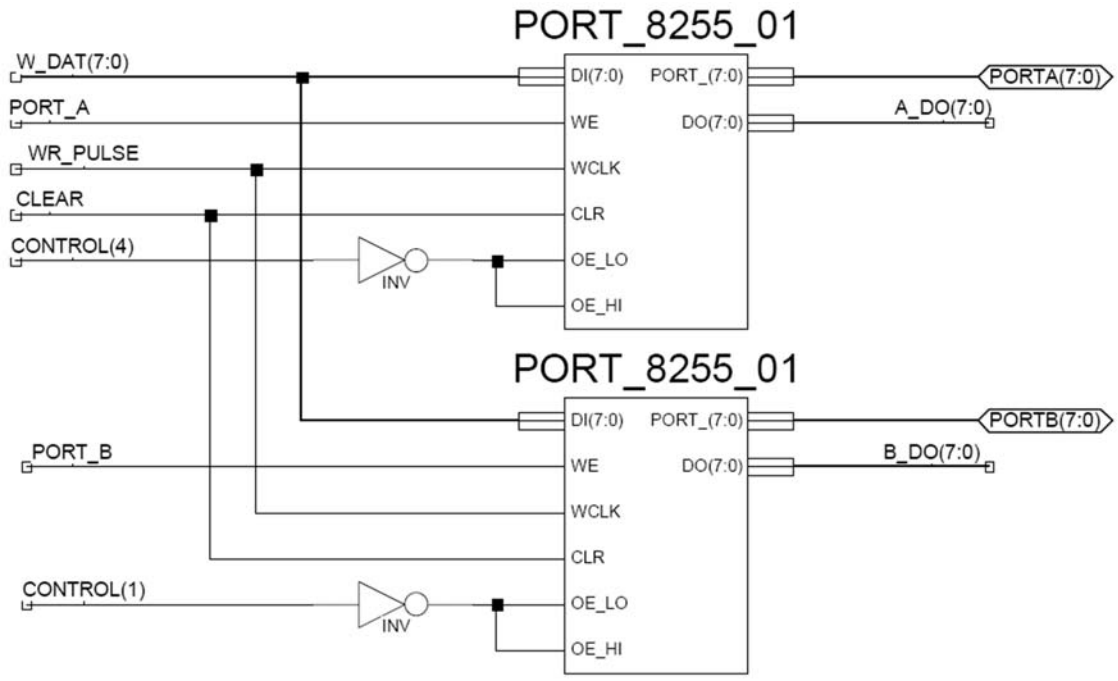
8255_01 port address decoder and selective addressing:



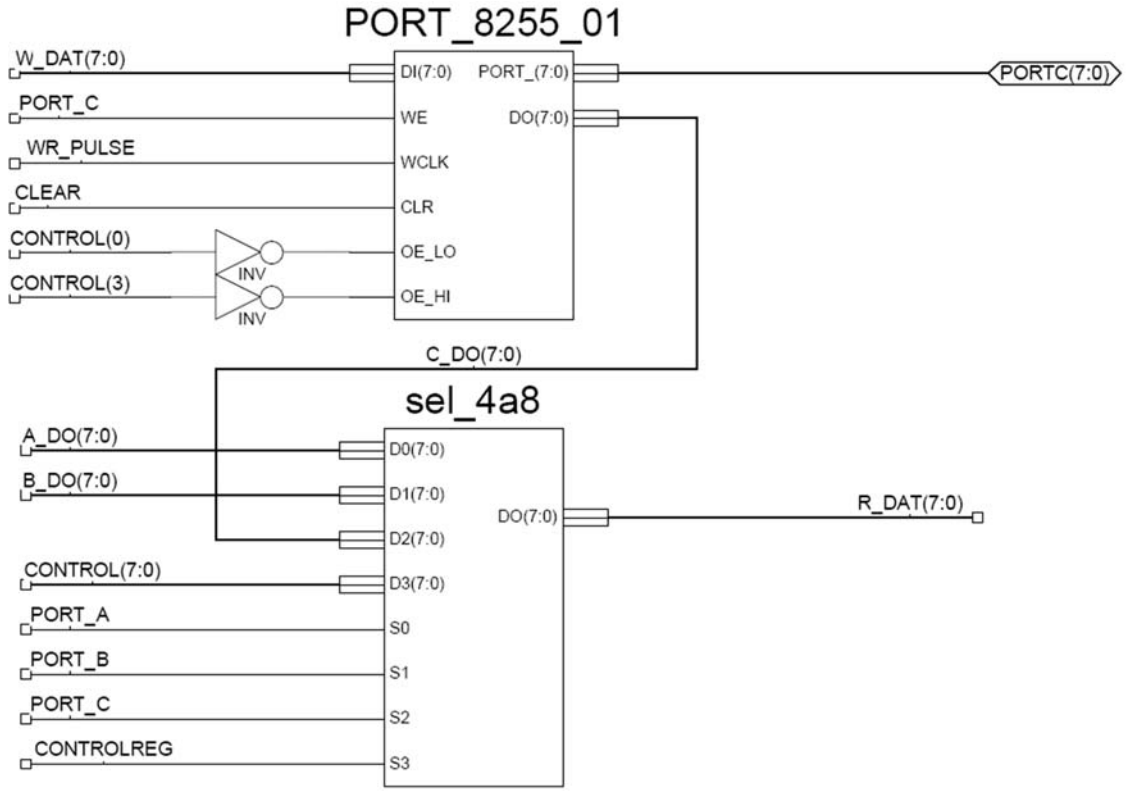
8255_01 mode register:



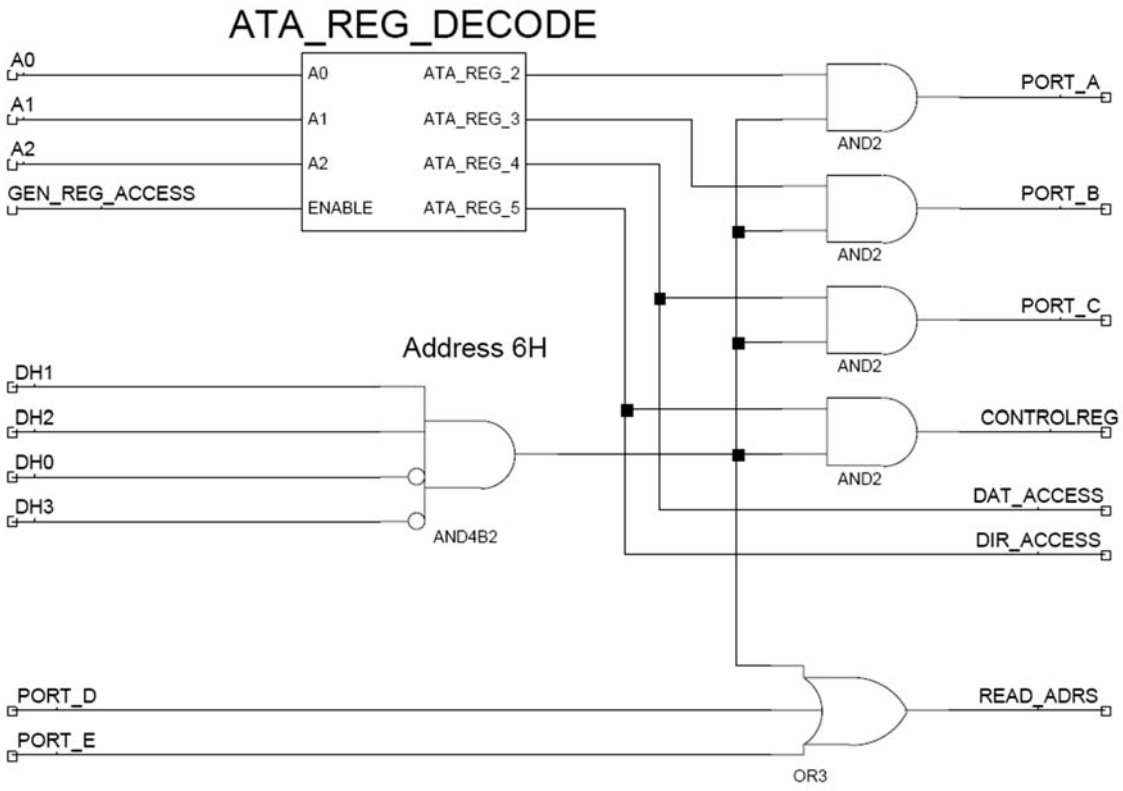
8255 ports A, B:



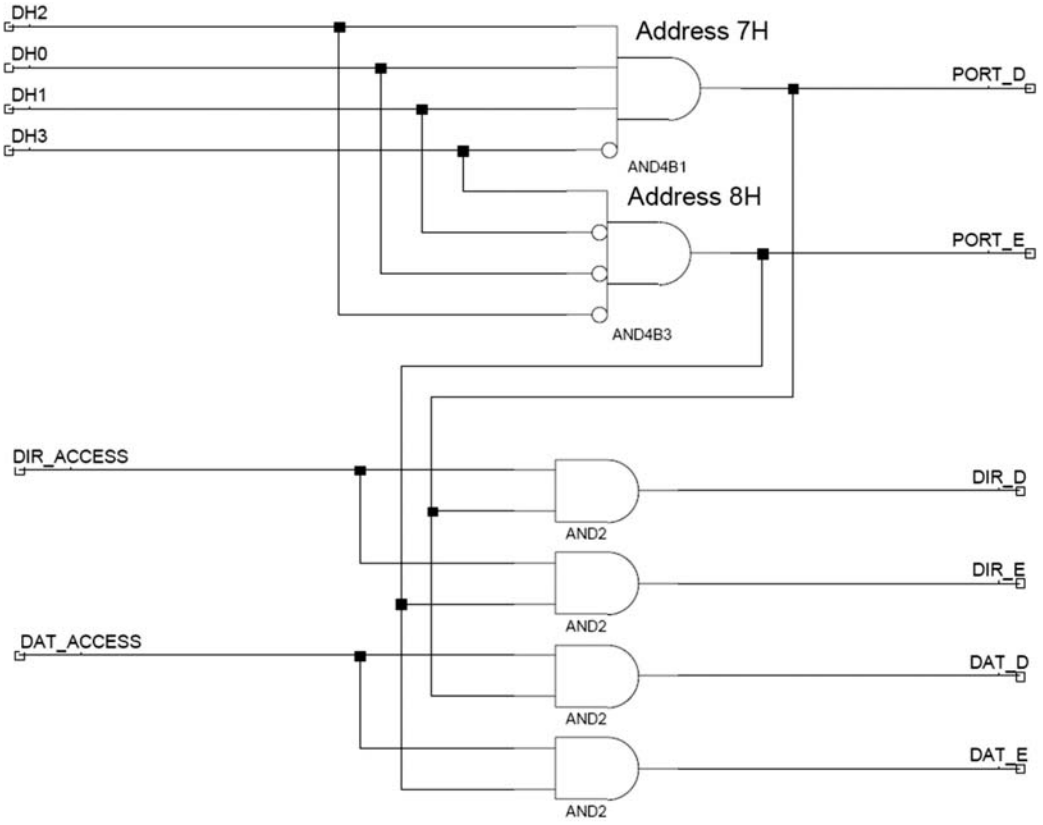
8255_01 port C and read data selector:



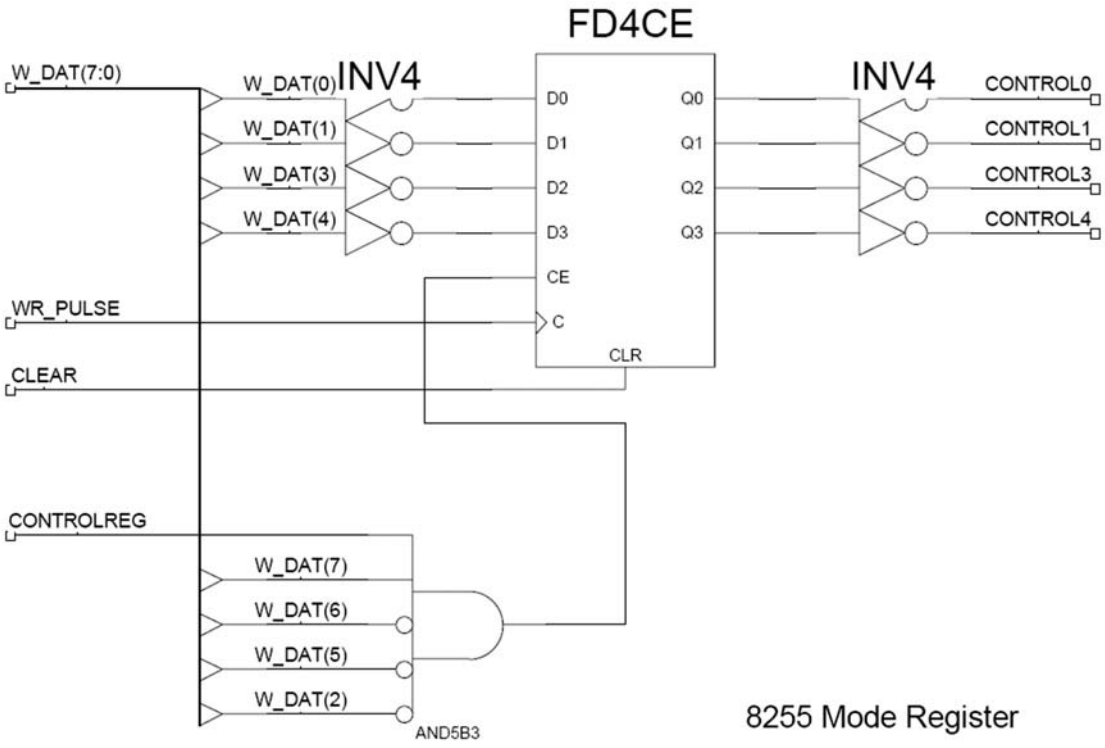
8255_02 port address decoder (1) and selective addressing (8255 ports):



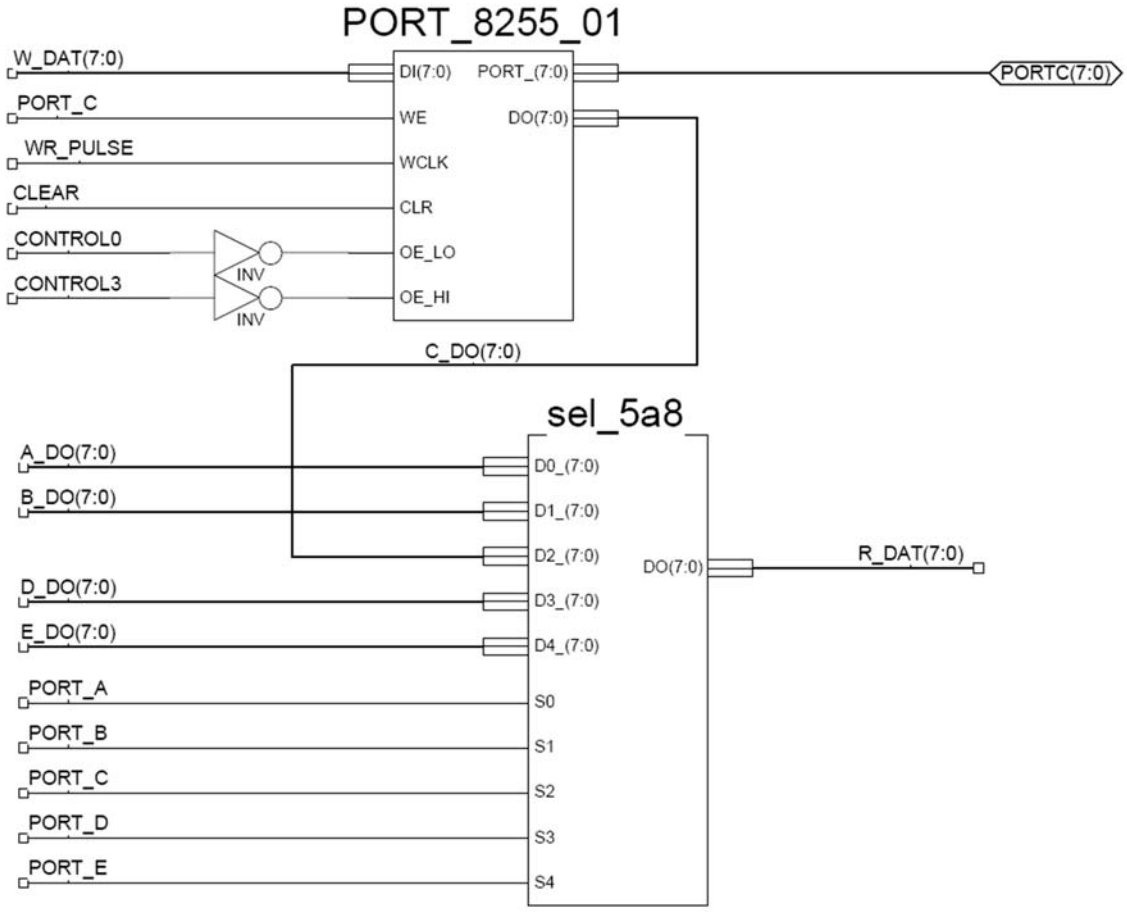
8255_02 port address decoder (2). Additional ports D, E:



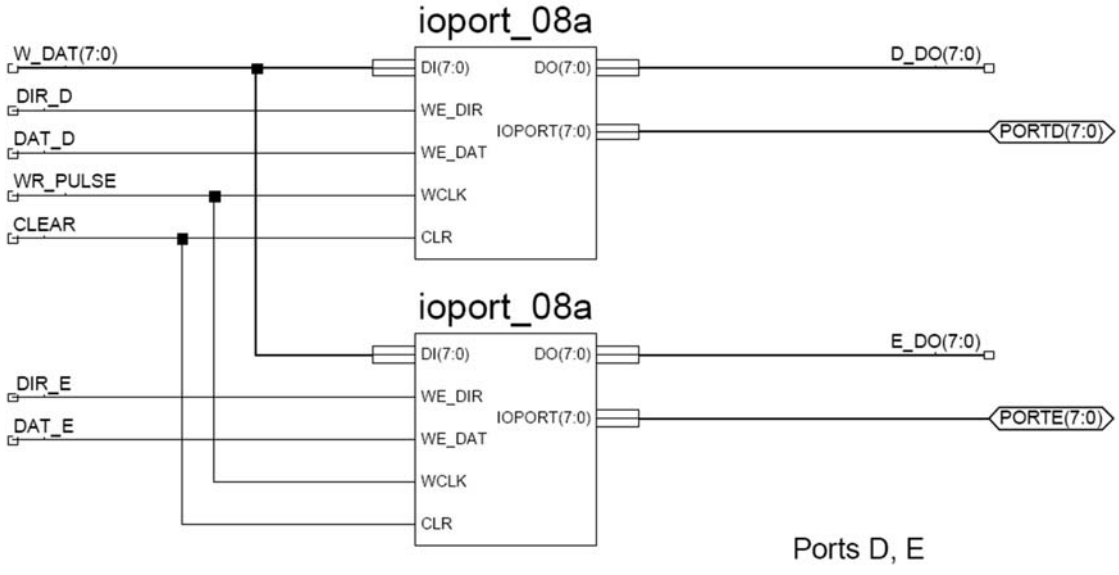
8255_02 mode register (simplified):



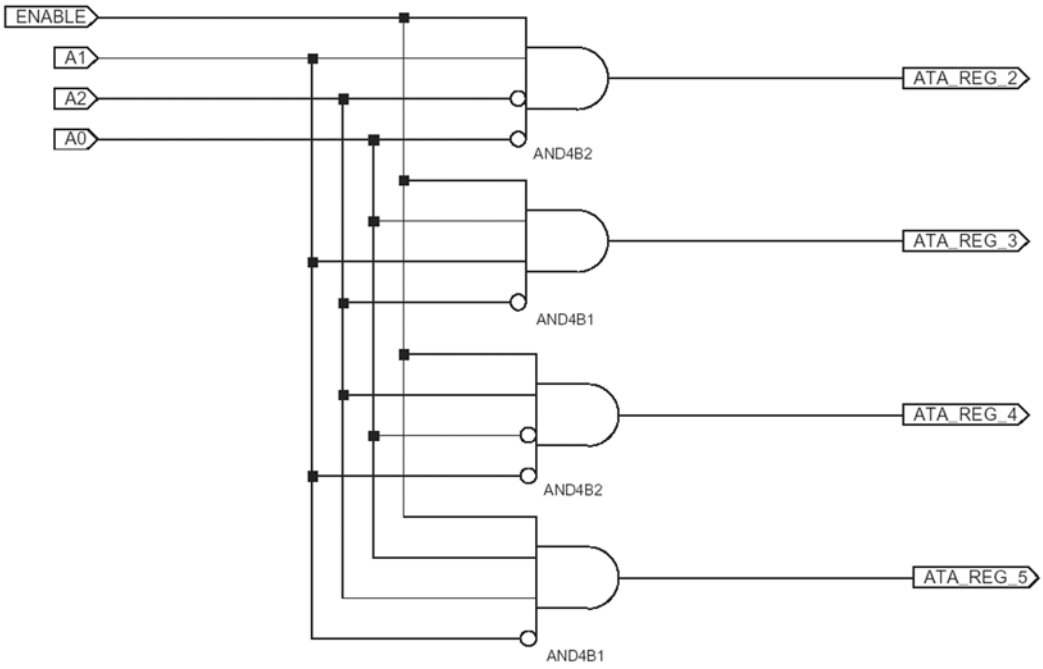
8255_02 port C and read data selector:



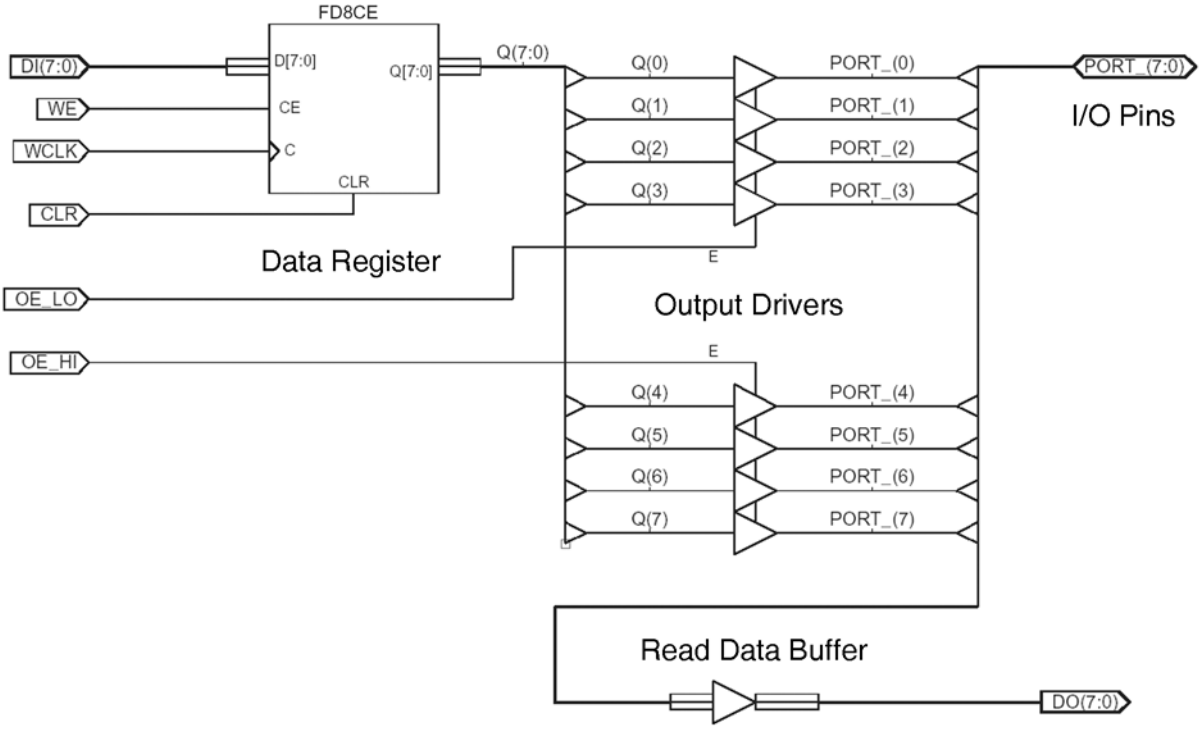
8255_02 aditional ports D and E:



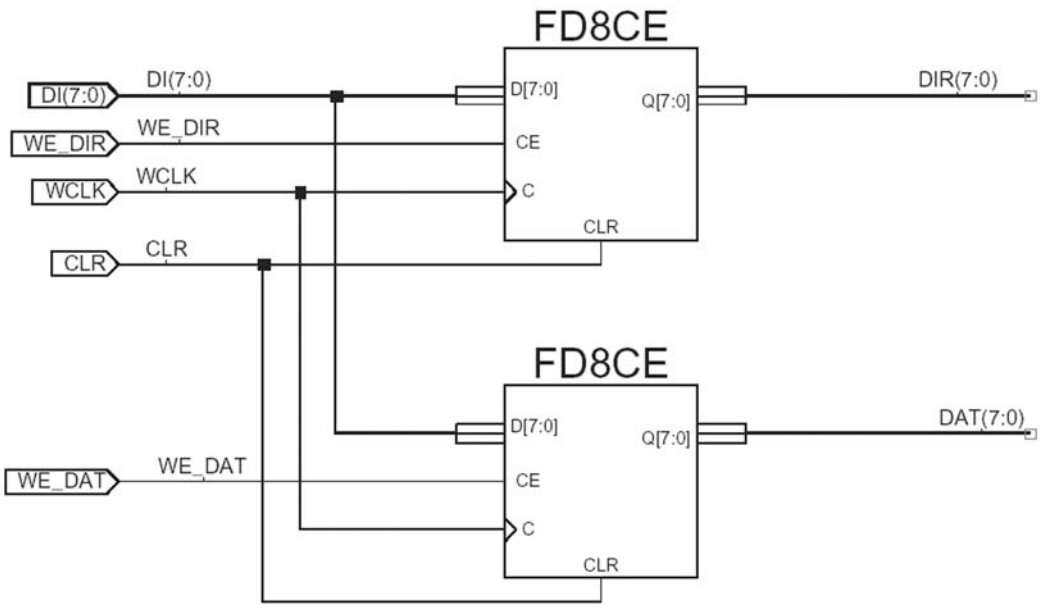
The ATA register address decoder:



One of the 8255 I/O ports (A, B, C):



Internals of a general-purpose I/O port (1). DIR and DAT registers (D, E):



Internals of a general-purpose I/O port (2): Drivers, buffers, and I/O pins (D, E):