ATA I/O Port Adapter 05a / 05ax

Programmer's Reference / Hardware Description

Release: 1.2 vom 19. 9. 06

Purpose:
Attachment of five general-purpose I/O ports (8 bits each) to a parallel ATA interface (fig. 1). Under program control, each of the 5 • 8 = 40 I/O lines can be used as an input or as an output.

ATA I/O port adapter 05a:
Restricted support of selective addressing. This circuit will fit into a Xlinx XC95108 CPLD (package PLCC 84).

ATA /O port adapter 05ax:
Complete support of selective addressing. This circuit requires at least a Xilinx XC95144 CPLD (or the like).

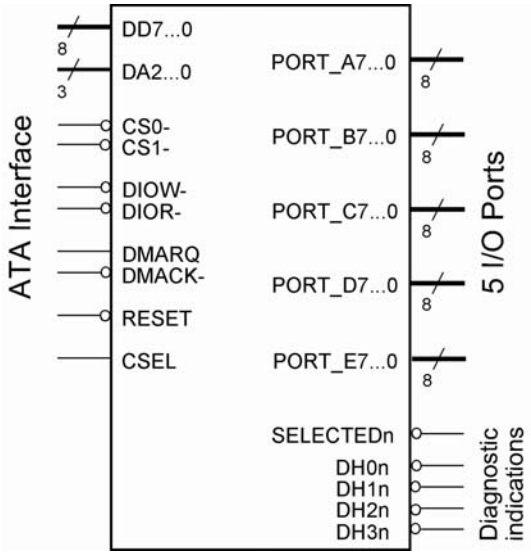


Fig. 1 ATA I/O adapter IC comprising five general-purpose I/O ports.

ATA signals supported:

- DD7...0 (8 bit data bus)
- CS0, CS1
- DA2, DA1, DA0
- DIOW, DIORD
- DMARQ, DMACK
- RESET
- CSEL

ATA signals not supported:

- DD15...8
- INTRQ, IORDY
- DASP, PDIAG, CSEL

Principles of I/O port operation
The I/O ports are similar to the typical I/O ports of well-known microcontroller families (Microchip PIC, Atmel AVR and the like). Each I/O port comprises a direction control register (DIR) and a data register (DAT). The DIR bit positions control the direction of the corresponding I/O signals (fig. 2):

- If the DIR bit is set to zero, the corresponding I/O pin is configured as an input, the pin driver being in high impedance state.
- If the DIR bit is set to one, the corresponding I/O pin is configured as an output. The potential (low or high) on the I/O pin corresponds to the bit in the DAT register.

After reset:
DIR = 00H (all I/O pins are in high impedance state), DAT = 00H.

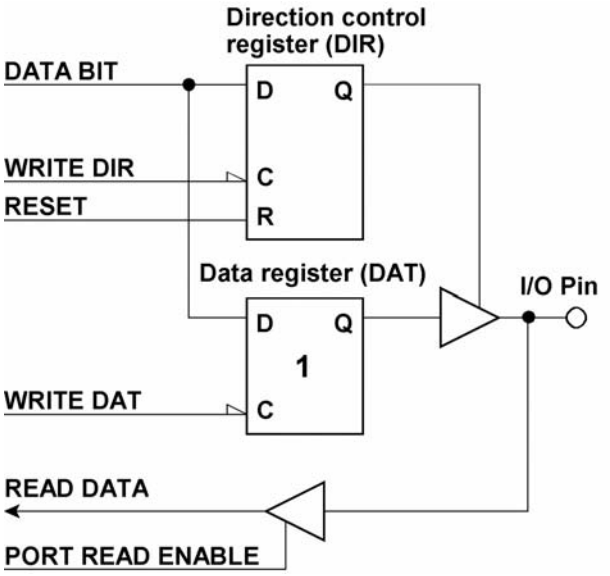


Fig. 2 Principal structure of an I/O bit position.

ATA device selection
Via the CSEL input, the I/O adapter can be configured as device 0 (master) or device 1 (slave):

- CSEL = 0: Master (Device 0),
- CSEL = 1: Slave (Devicve 1).

Typically, CSEL will be wired to Low or High potential or connected to the CSEL line of the ATA interface (Cable Select).

I/O addressing
Each of the five ports (A... E) has its own port address in the DH register (fig. 3, table 1). Within each port, the data register (DAT) as well as the direction control register (DIR) are to be addressed (table 2).

7	6	5	4	3	2	1	0
-	-	-	DEVICE	I/O Port Selection (Port Address)			

Fig. 3 DH register content.

DH register bits 3... 0	I/O port
1H	Port A
2H	Port B
3H	Port C
4H	Port D
5H	Port E
all other values	no effect

Table 1 I/O Port addressing via DH register.

CS		Register Address DA				Register	Legacy ATA Ports			
1-	0-	2	1	0	Hex		1	2	3	4
1	0	1	0	0	4	Data register (DAT)	1F4	174	1EC	16C
1	0	1	0	1	5	Direction control register (DIR)	1F5	175	1ED	16D
1	0	1	1	0	6	Device selection and port address register (DH)	1F6	176	1EE	16

Table 2 Register addressing within a selected I/O port. Read accesses to either DAT or DIR addresses will read back the potentials on the I/O pins.

I/O port selection
Writing into a register of or reading from an I/O port requires two steps:

1. Select the ATA device and the I/O port by writing into the DH register.

2. Write to or read from either the data register or the direction control register of the selected port.

A port address loaded into the DH register will be retained. Therefore, if an already selected port is to be accessed, step 1 could be skipped.

Write operations
A write access to one of the ATA port addresses according to table 2 will write the data byte into the DH register or into the data register or the direction control register of the selected I/O port. A write access with any other address has no effect upon the I/O adapter.

*Read operation*s
Contrary to the operation of some microcontroller ports (like those of the Atmel AVR controllers), only the potentials (low or high) on the I/O pins can be read back. A read access to the direction control register or to the data register will return the potentials on the corresponding I/O pins. If a read access is directed to the DH register or to a port address which does not belong to the allocated range of addresses (selective addressing), the adapter will not act upon the data bus. Thus, the ATA host adapter will deliver a value FFH. The result of read operations with other addresses is not defined.

Writing into a register of an I/O port requires two steps:

1. Select the ATA device and the I/O port by writing into the DH register.

2. Perform a read access to either the data register or the direction control register of the selected port.

A port address loaded into the DH register will be retained. Therefore, if an already selected port is to be accessed, step 1 could be skipped.

Selective addressing
Selective addressing is a provision to permit attaching more than one ATA I/O adapter at one interface cable. With this feature implemented, the adapter will only react on particular port addresses.

- The ATA I/O port adapter 05ax will react only on the port addresses shown in table 1 (1H...5H).
- The ATA I/O port adapter 05a1 will react only on port addresses 0H...5H.

Notes:

1. The selective addressing feature can be omitted if the adapter will be the only ATA I/O circuit at the interface cable.

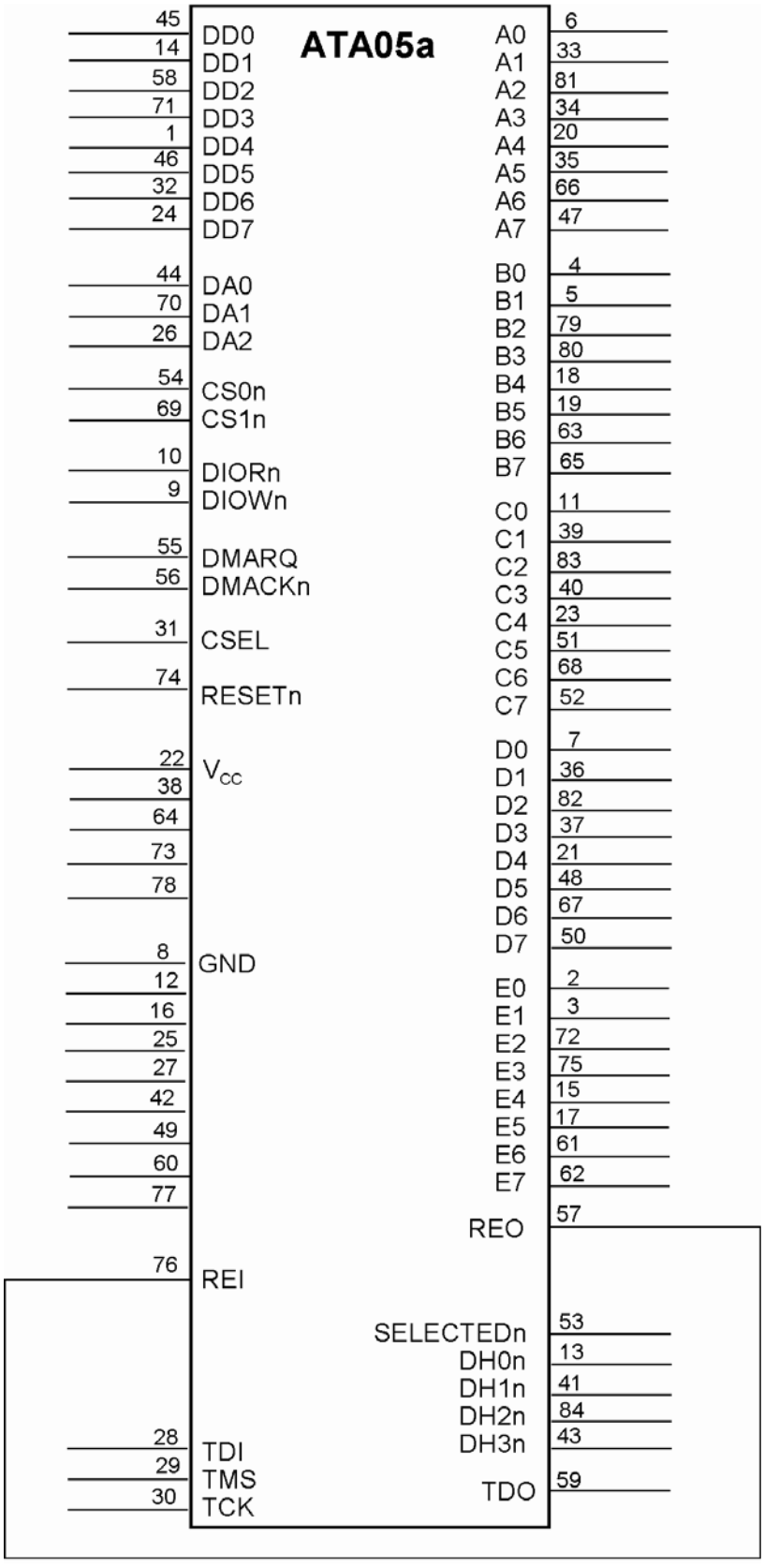
2. If selective addressing is not to be implemented at all, the READ_ADRS input of the ATA I/O front end is to be connected to High potential.

Diagnostic indications:
These signals are provided to drive LEDs (active low). The LEDs will show:

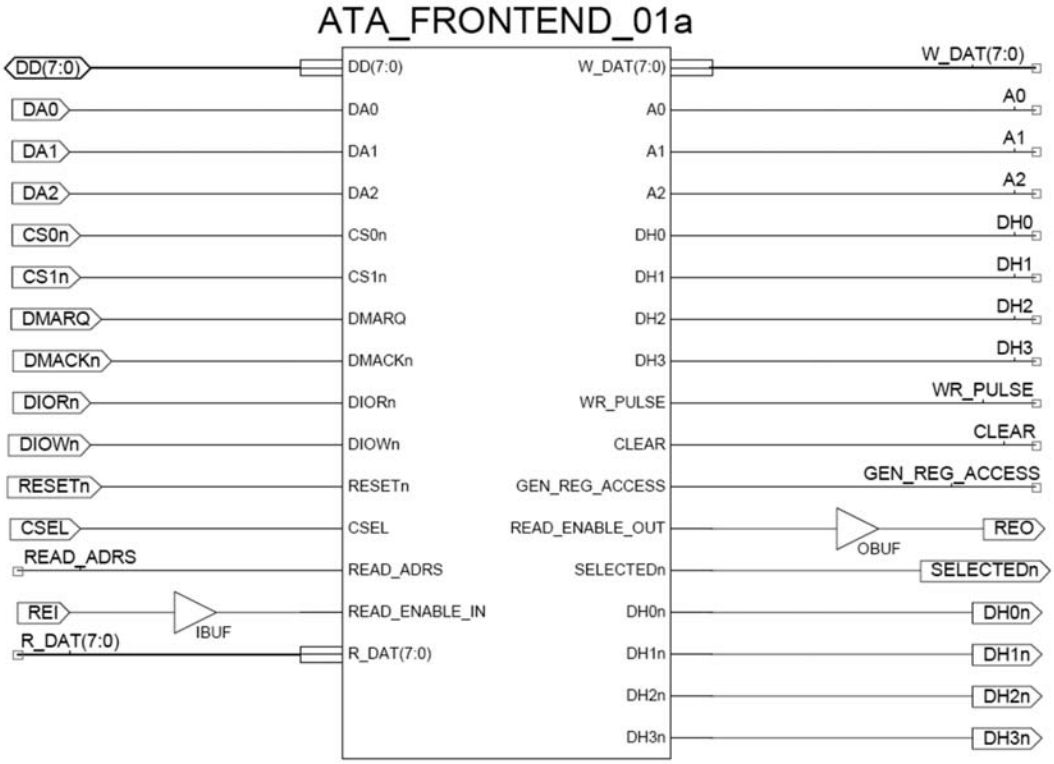
- Whether the adapter has been selected.
- The port address field of the DH Register (DH3...0).

ATA I/O port adapter 05a pinout:

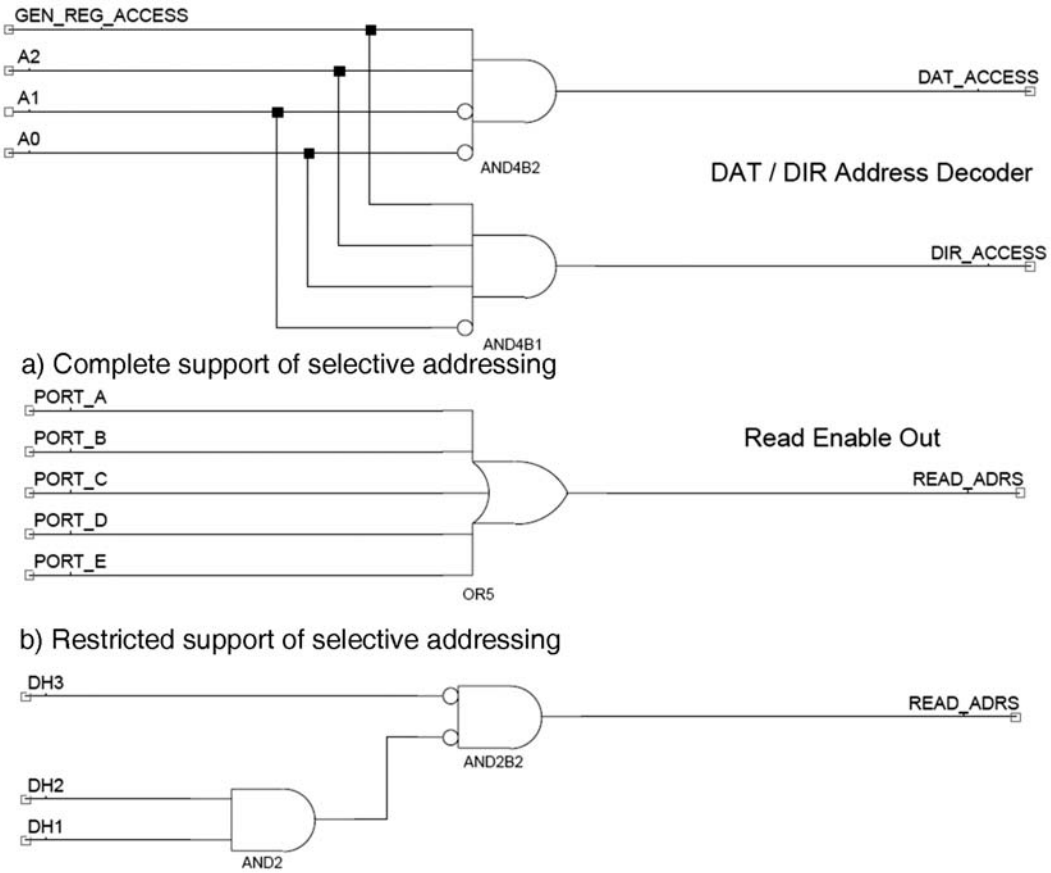
Pin No.	Signal Name	Pin No.	Signal Name
1	DD<4>	43	DH3n
2	PORTE<0>	44	DA0
3	PORTE<1>	45	DD<0>
4	PORTB<0>	46	DD<5>
5	PORTB<1>	47	PORTA<7>
6	PORTA<0>	48	PORTD<5>
7	PORTD<0>	49	GND
8	GND	50	PORTD<7>
9	DIOWn	51	PORTC<5>
10	DIORn	52	PORTC<7>
11	PORTC<0>	53	SELECTEDn
12	PGND	54	CS0n
13	DH0n	55	DMARQ
14	DD<1>	56	DMACKn
15	PORTE<4>	57	REO
16	GND	58	DD<2>
17	PORTE<5>	59	TDO
18	PORTB<4>	60	GND
19	PORTB<5>	61	PORTE<6>
20	PORTA<4>	62	PORTE<7>
21	PORTD<4>	63	PORTB<6>
22	VCC	64	VCC
23	PORTC<4>	65	PORTB<7>
24	DD<7>	66	PORTA<6>
25	PGND	67	PORTD<6>
26	DA2	68	PORTC<6>
27	GND	69	CS1n
28	TDI	70	DA1
29	TMS	71	DD<3>
30	TCK	72	PORTE<2>
31	CSEL	73	VCC
32	DD<6>	74	RESETn
33	PORTA<1>	75	PORTE<3>
34	PORTA<3>	76	REI
35	PORTA<5>	77	PGND
36	PORTD<1>	78	VCC
37	PORTD<3>	79	PORTB<2>
38	VCC	80	PORTB<3>
39	PORTC<1>	81	PORTA<2>
40	PORTC<3>	82	PORTD<2>
41	DH1n	83	PORTC<2>
42	GND	84	DH2n


ATA05a
45 DD0
14 DD1
58 DD2
71 DD3
1 DD4
46 DD5
32 DD6
24 DD7
44 DA0
70 DA1
26 DA2
54 CS0n
69 CS1n
10 DIORn
9 DIOWn
55 DMARQ
56 DMACKn
31 CSEL
74 RESETn
22 38 64 73 78 Vcc
8 12 16 25 27 42 49 60 77 GND
76 REI
28 TDI
29 TMS
30 TCK
A0 6
A1 33
A2 81
A3 34
A4 20
A5 35
A6 66
A7 47
B0 4
B1 5
B2 79
B3 80
B4 18
B5 19
B6 63
B7 65
C0 11
C1 39
C2 83
C3 40
C4 23
C5 51
C6 68
C7 52
D0 7
D1 36
D2 82
D3 37
D4 21
D5 48
D6 67
D7 50
E0 2
E1 3
E2 72
E3 75
E4 15
E5 17
E6 61
E7 62
REO 57
SELECTEDn 53
DH0n 13
DH1n 41
DH2n 84
DH3n 43
TDO 59

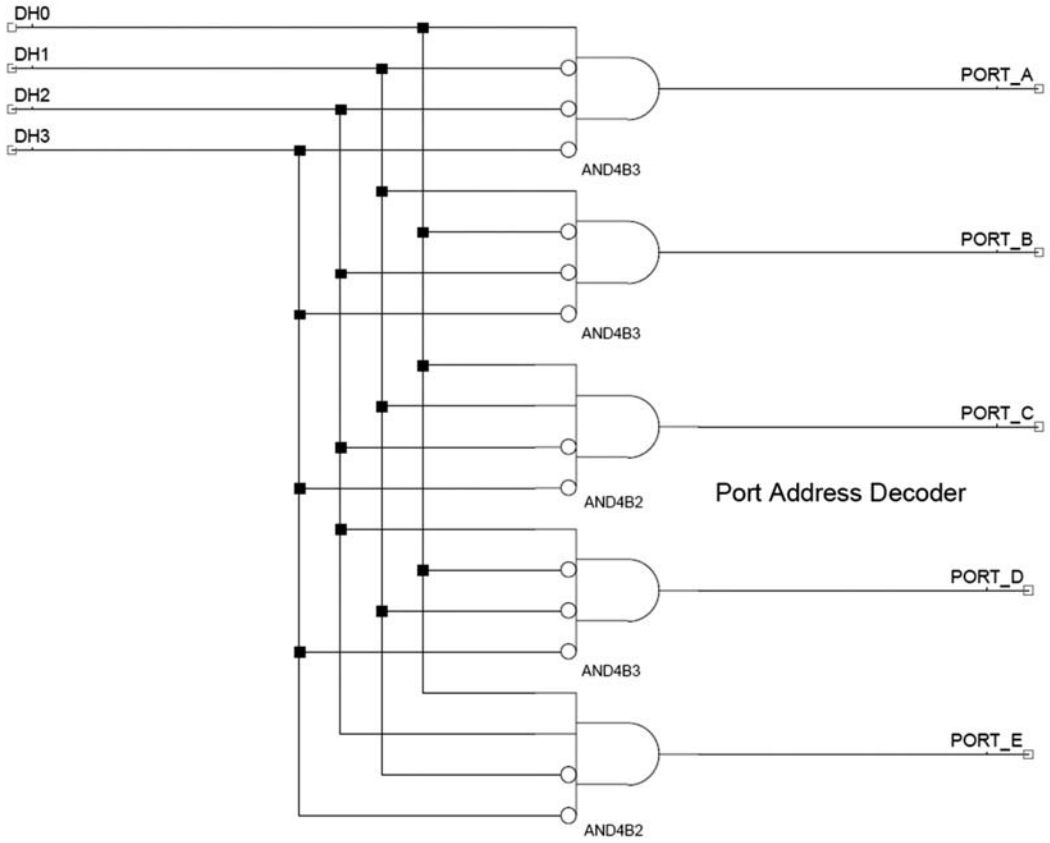
The ATA interface:



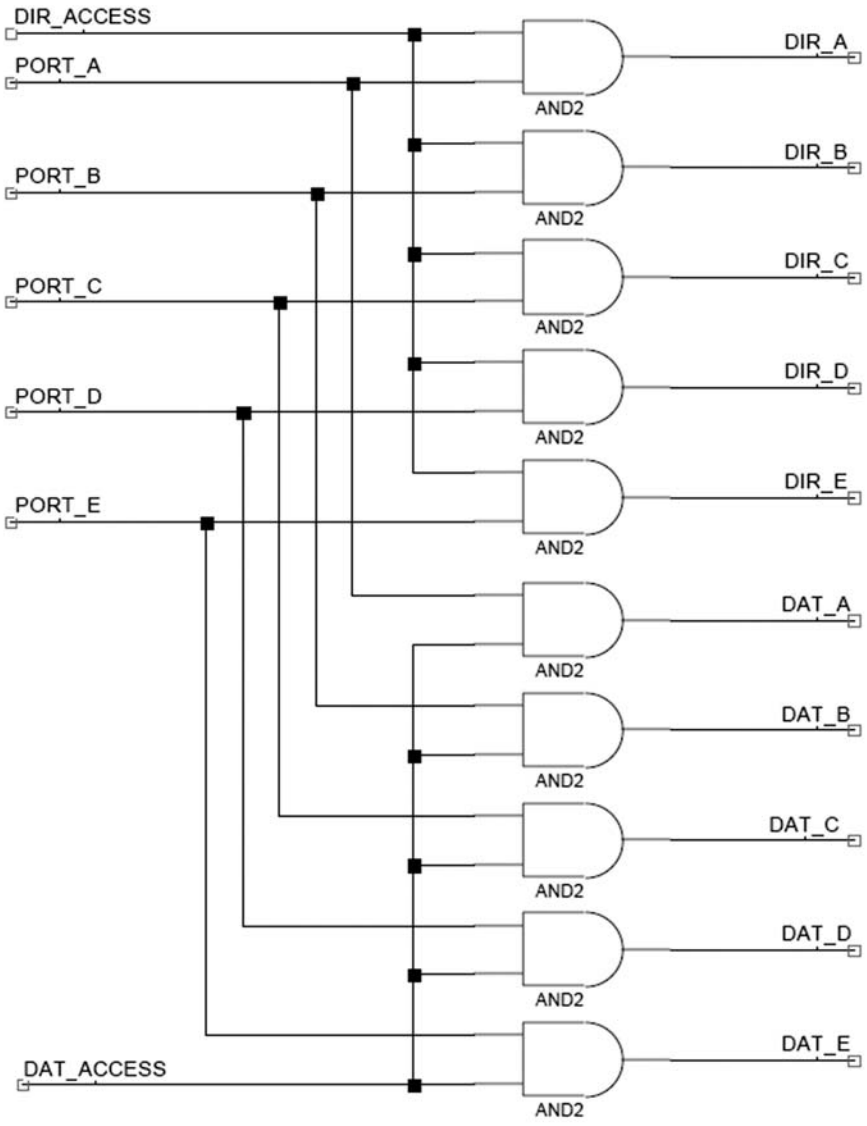
DAT / DIR address decoder and selective addressing:



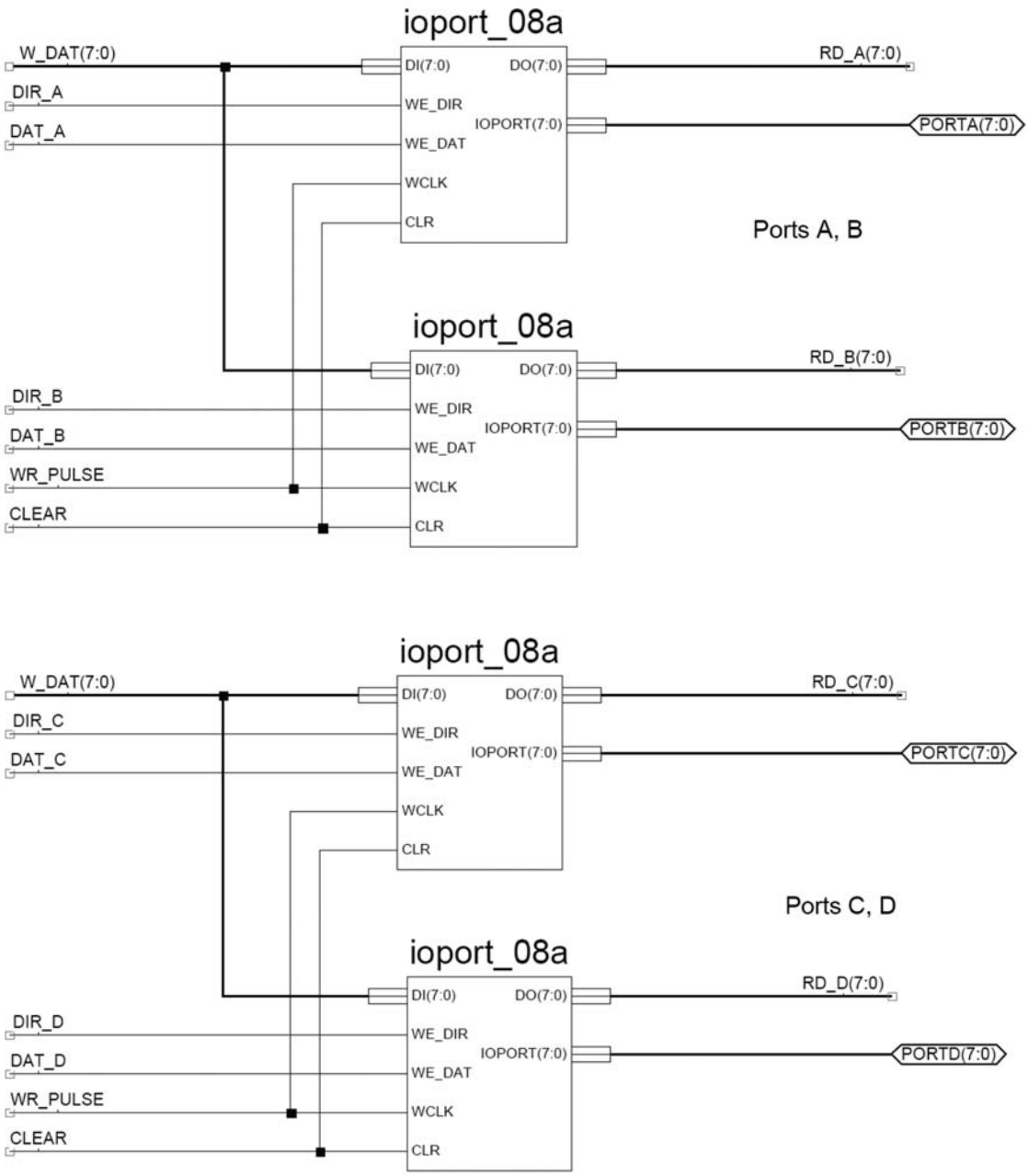
Port address decoder:



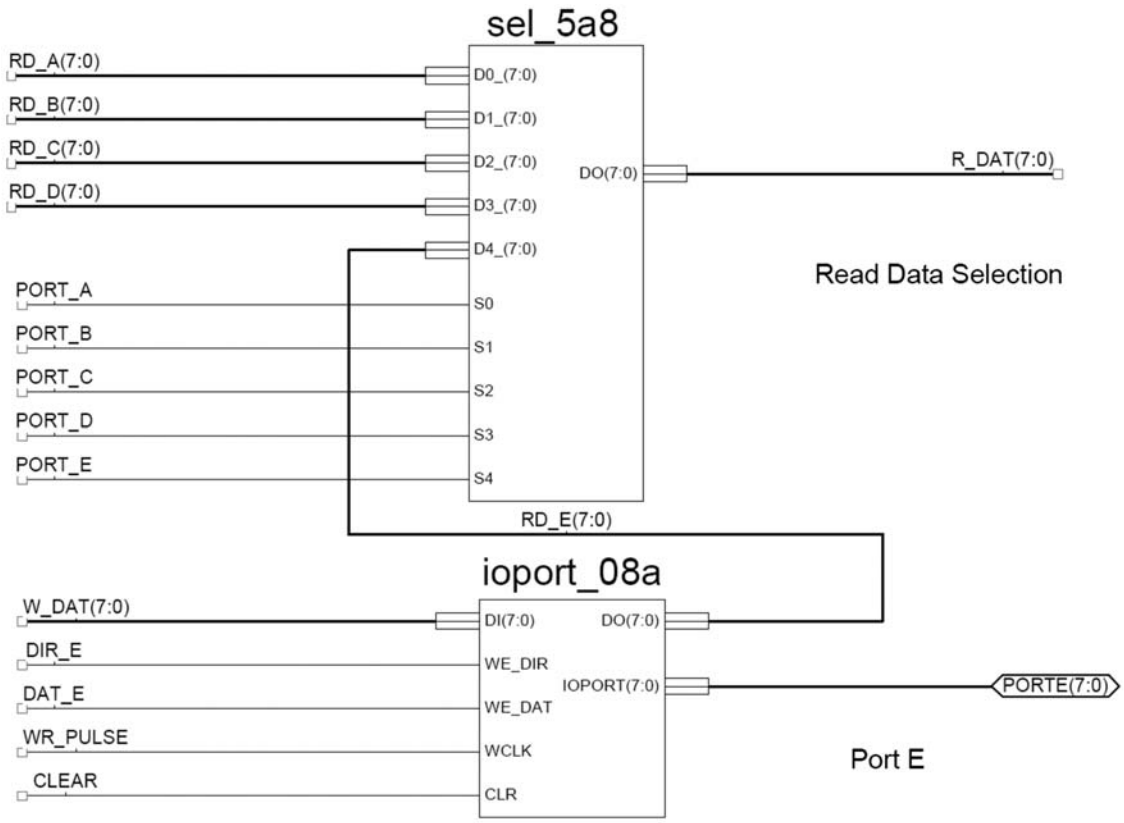
Write enable signals to all of the DIR and DAT registers:



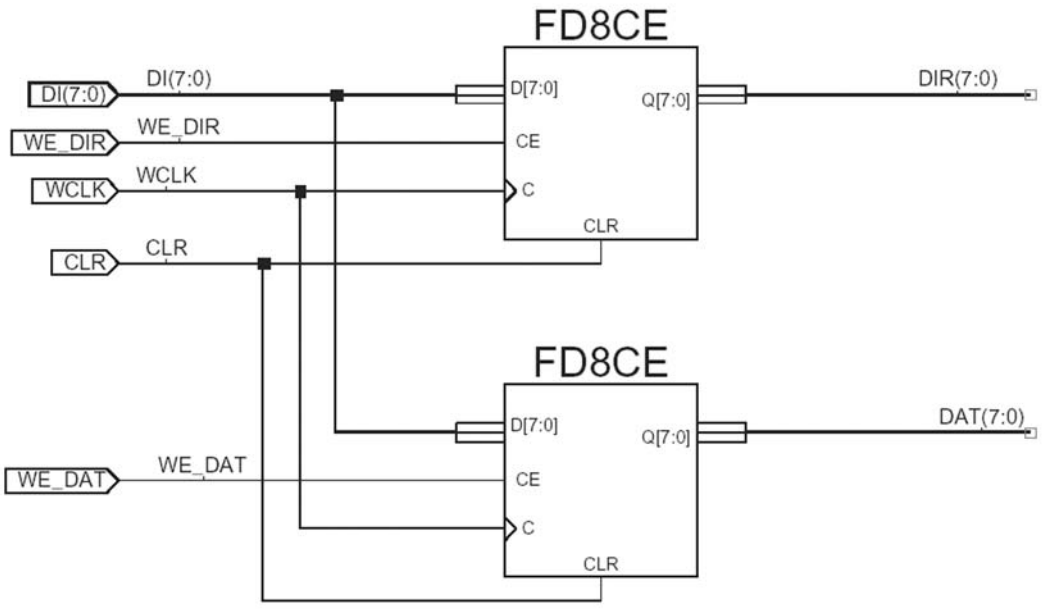
I/O ports A to D:



Read data selector and I/O port E:



Internals of an I/O port (1): DIR and DAT registers:



Internals of an I/O port (2): Drivers, buffers, and I/O pins: