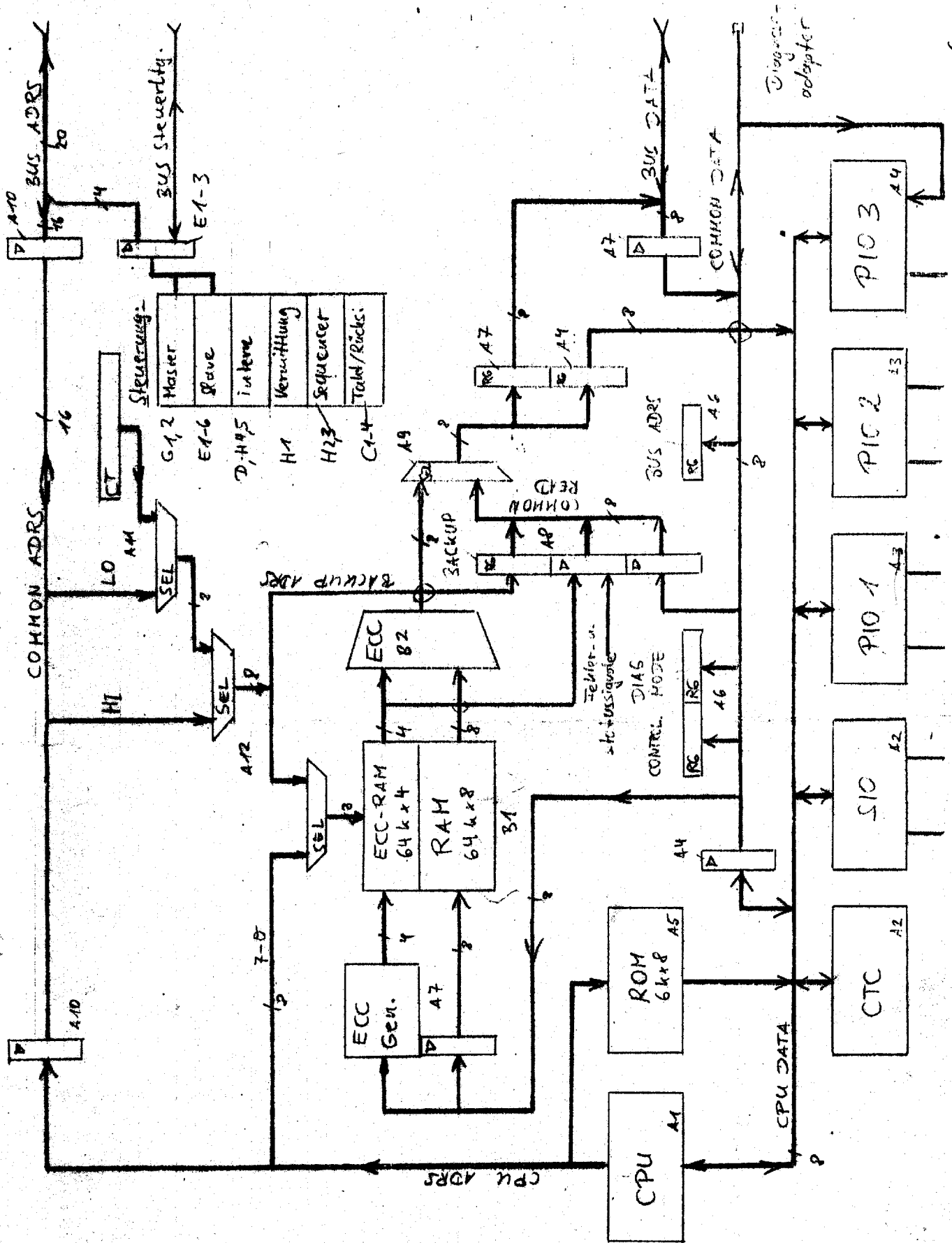


System 386M ADVANCED SINGLE BOARD COMPUTER (SBC/64k)

- 1.4.86

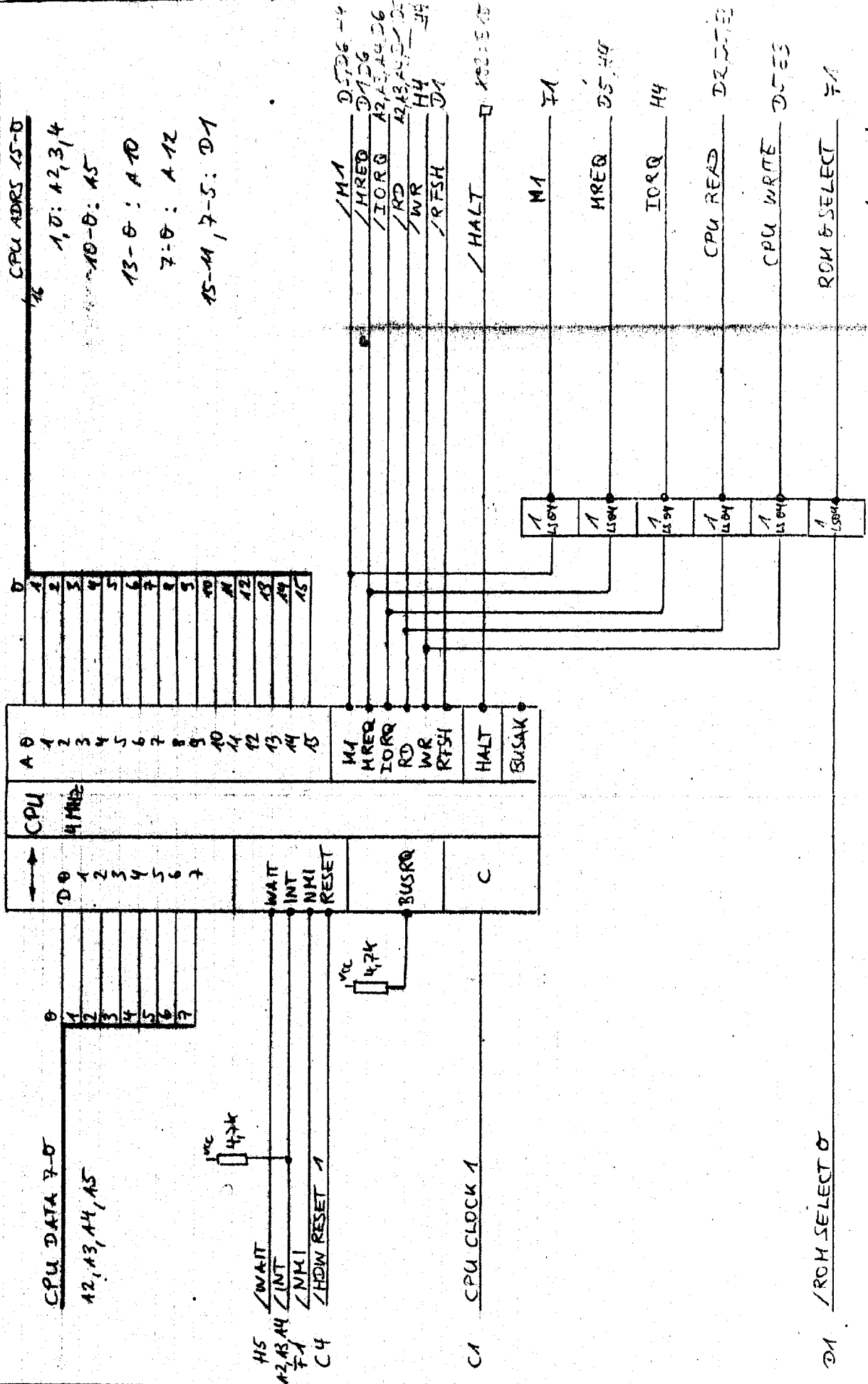


E - A - Anschlüsse

D18-1178

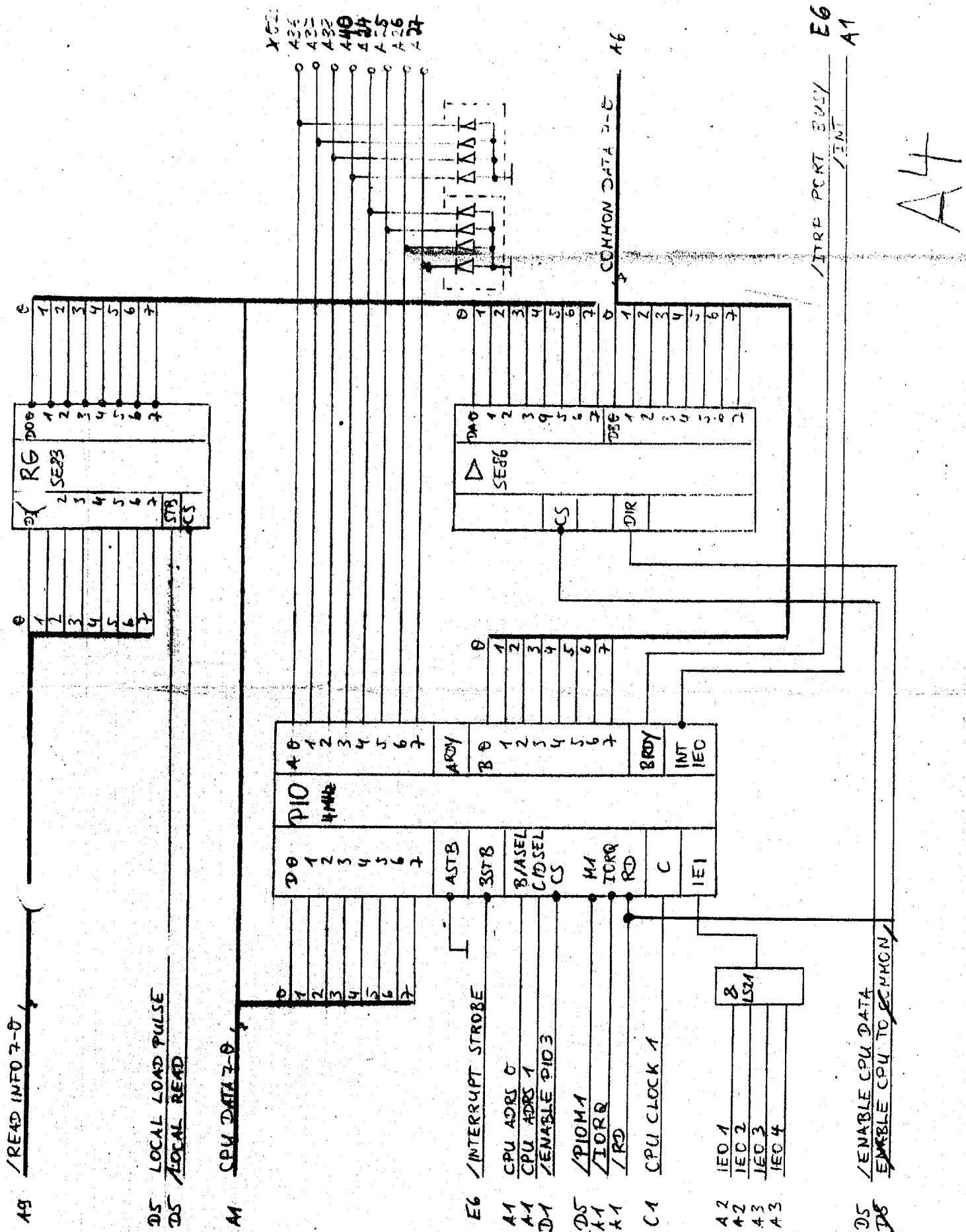
Ue

①



AA

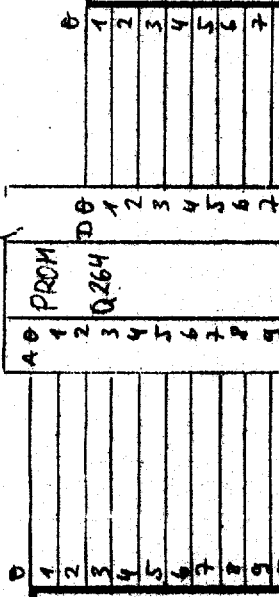
D1 / ROM SELECT 0



14.4.86
M4

A1 CPU ADDR 10-0

CPU DATA 7-0

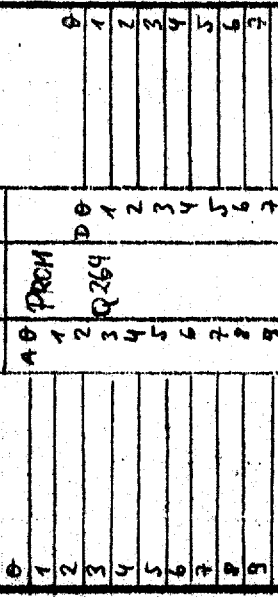


DM /ROM SELECT 0

Vcc

OE

CS

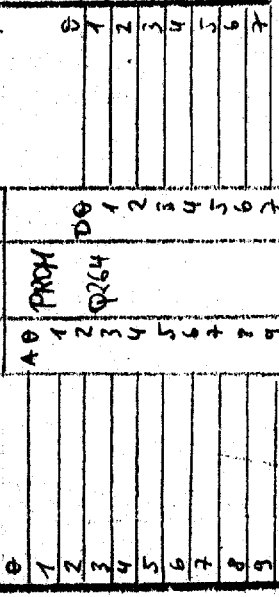


DM /ROM SELECT 1

Vcc

OE

CS



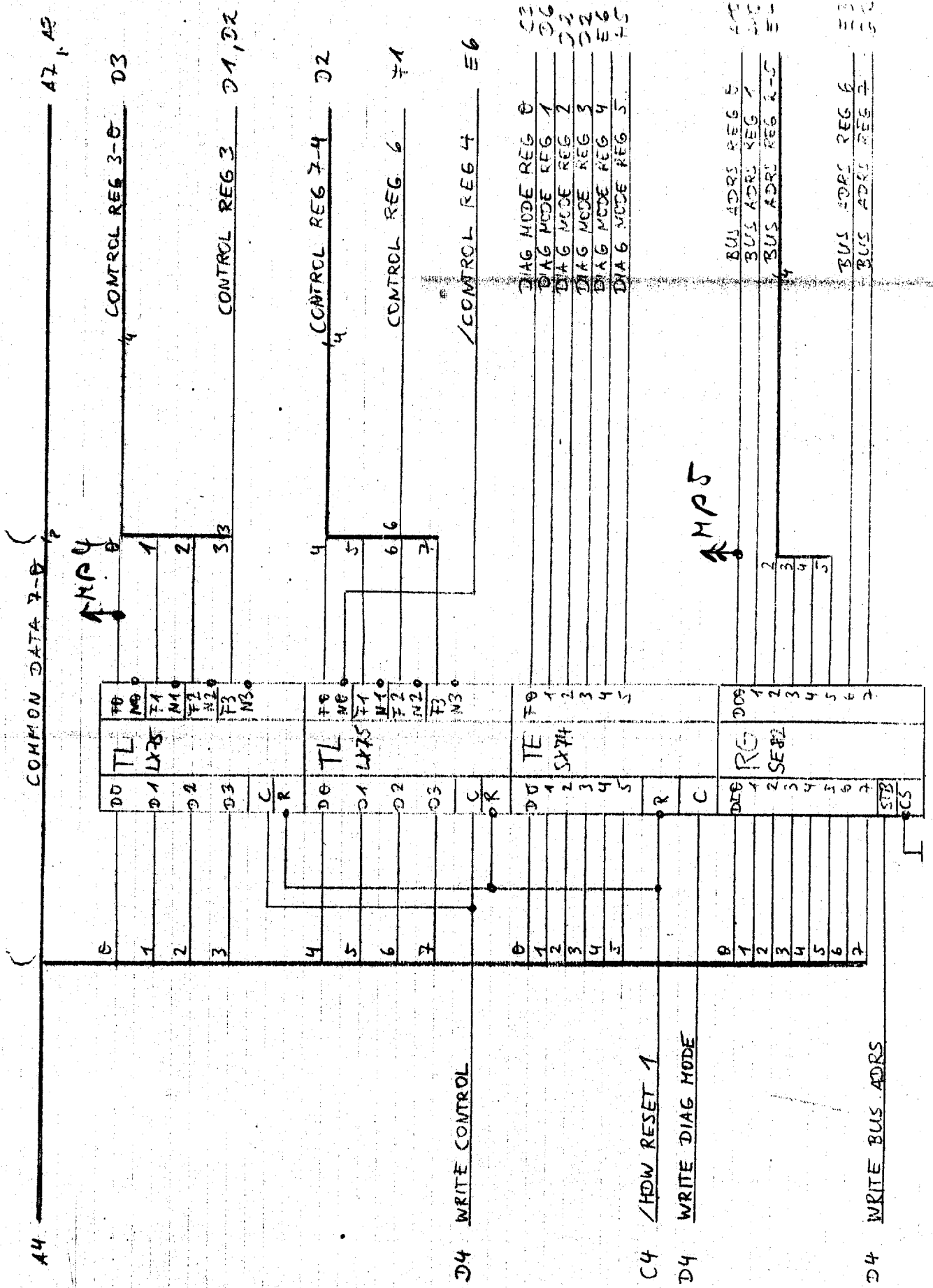
DM /ROM SELECT 2

Vcc

OE

CS

A5

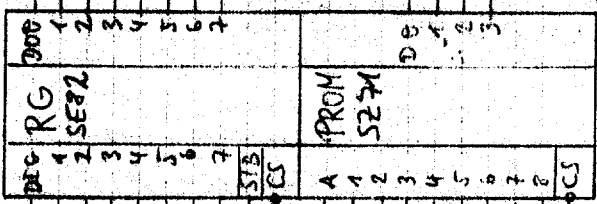


A6

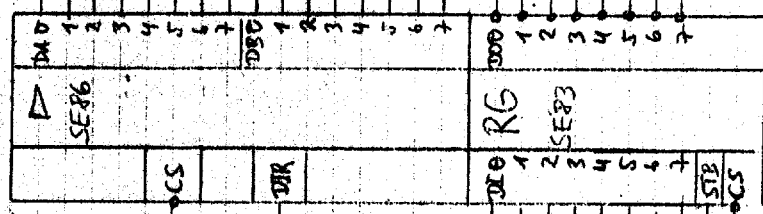
A6 COMMON DATA 7-0

COMMON DATA 8
1
2
3
4
5
6
7

RAMDI 4-8 31
1
2
3
4
5
6
7



RAMDI 4-8 31
1
2
3
4
5
6
7



D5 /ENABLE BUS DATA

D5 /ENABLE COMMON TO BUS

A9 /READ INFO 7-0

BUS DATA 8
1
2
3
4
5
6
7

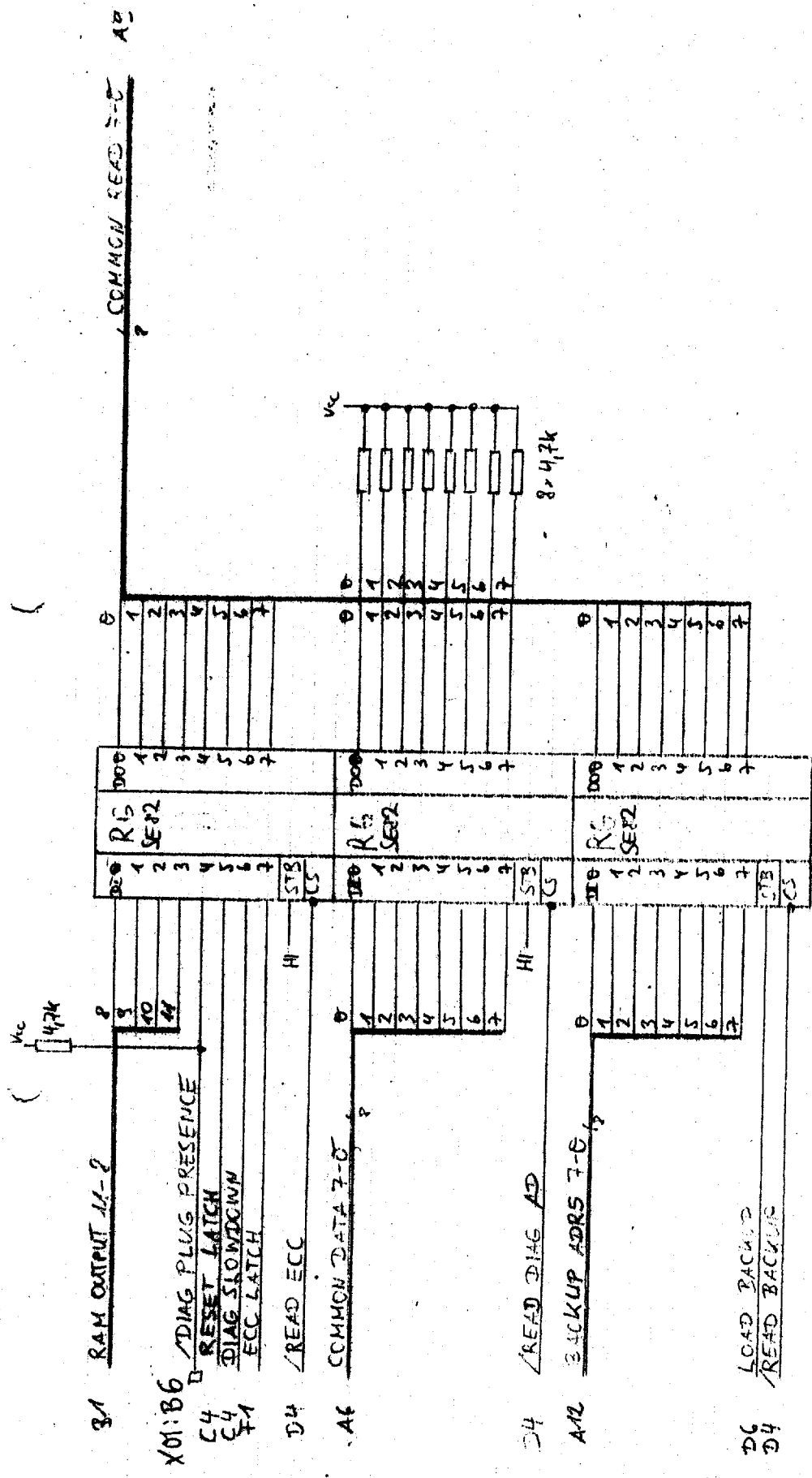
D5 /SLAVE LOAD PULSE
D5 /SLAVE READ

D2 ECC DATA ACCESS

A1
A2
A3
A4
A5
A6
A7
A8

A1
A2
A3
A4
A5
A6
A7
A8

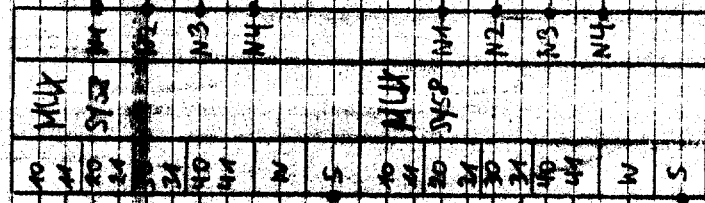
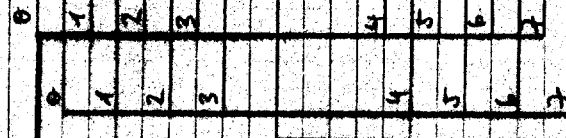
A7



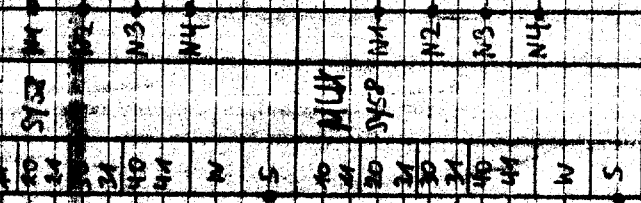
3A RAM OUTPUT 11-2
 X01:86
 C4 DIAG PLUG PRESENCE
 C4 RESET LATCH
 7-1 DIAG SLOWDOWN
 D4 /READ ECC
 A6 COMMON DATA 7-0
 D4 /READ DIAG AD
 A12 BACKUP ADRS 7-0
 D6 /LOAD BACKUP
 D4 /READ BACKUP

COMMON READ 7-0 A8

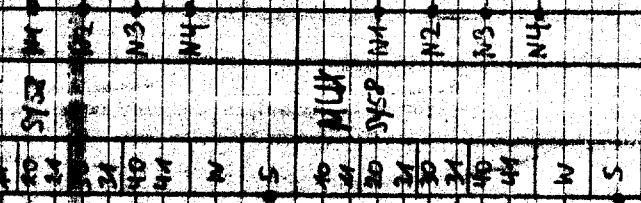
82 RAM DATA 7-0



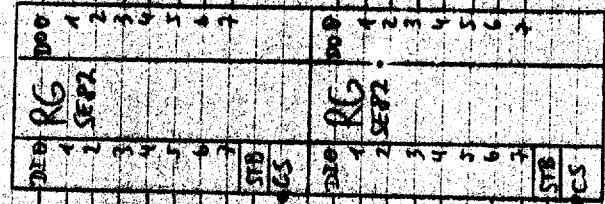
83 COMMON READ 7-0



84 SPECIAL READ

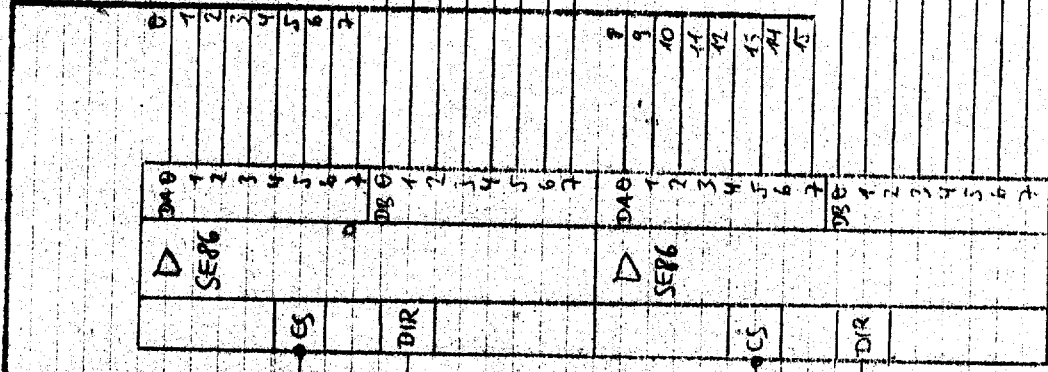


04 CPU ADRES 15-0



COMMON ADRES 15-0

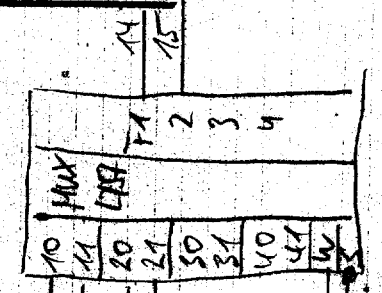
2-0: D4
 7-0: A4
 11-8: A12
 15-12: D3
 15: E6



BUS ADRES 0
 1
 2
 3
 4
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 6
 7

103
 A1
 31
 A2
 13
 33
 A4
 24
 35

04 MASTER BUSY



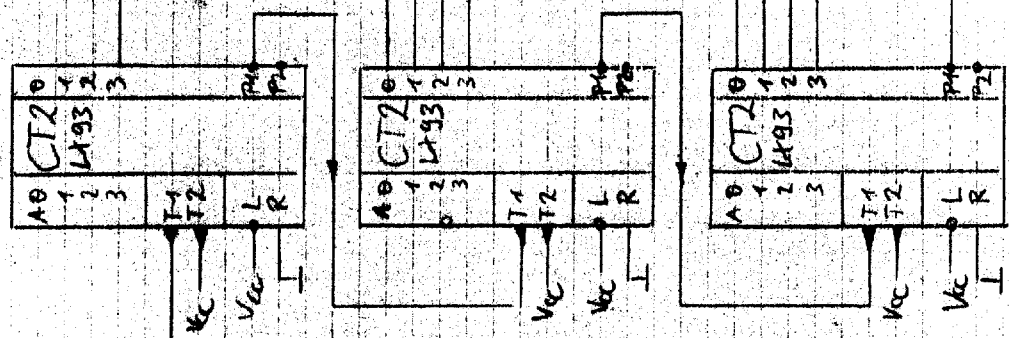
CPU ADRES 14
 BUS ADRES REG 0
 CPU ADRES 11
 BUS ADRES REG 1

MASTER BUSY

15.7.86
[Signature]

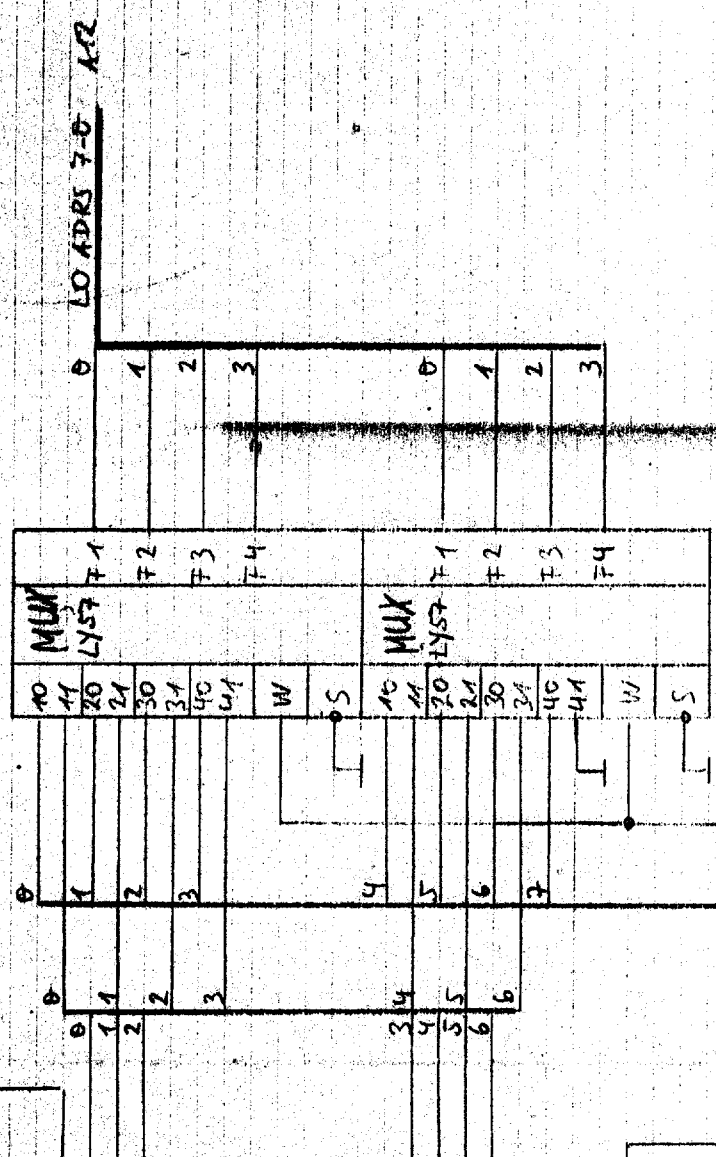
AD

RESH CTR 3 C3
RESH CTR 4 C3



C2 REFRESH CLOCK

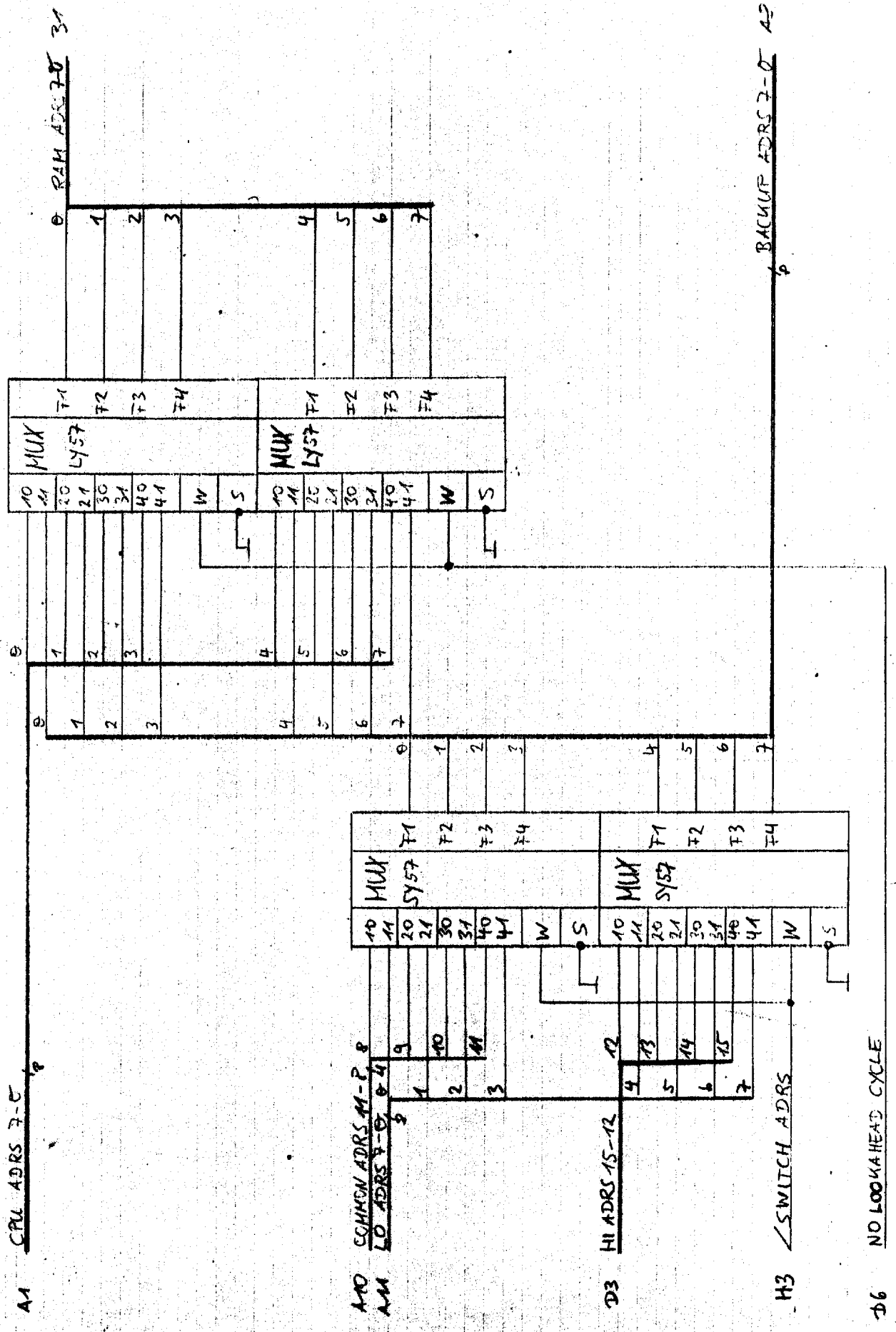
A0 COMMON ADRS 7-6
H1 REFRESH CYCLE



LO ADRS 7-0 A/R2

RESH CTR CARRY C3

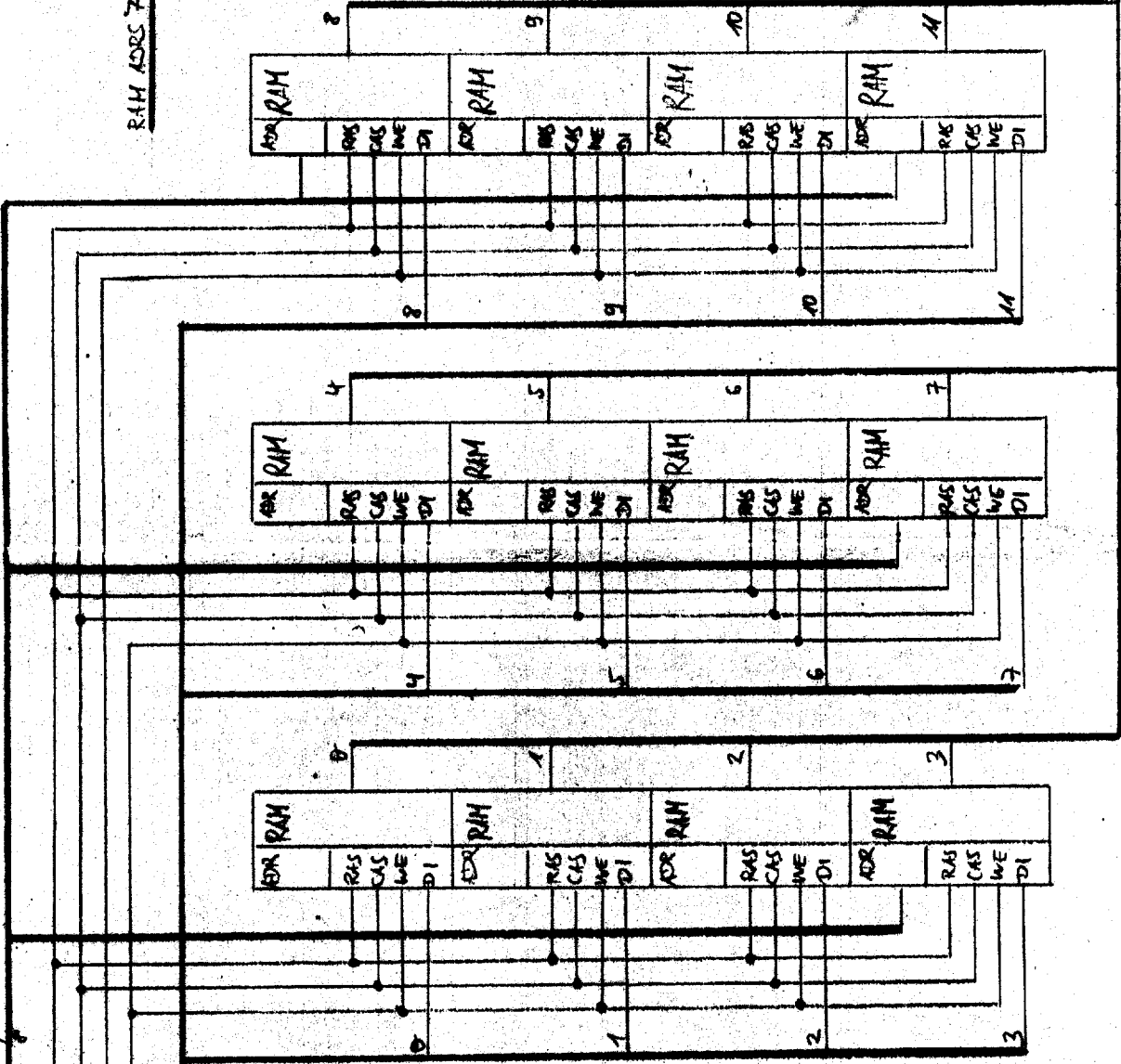
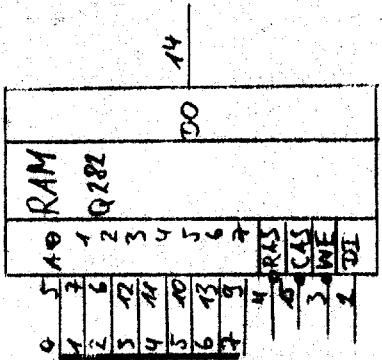
AM



Detail RAM

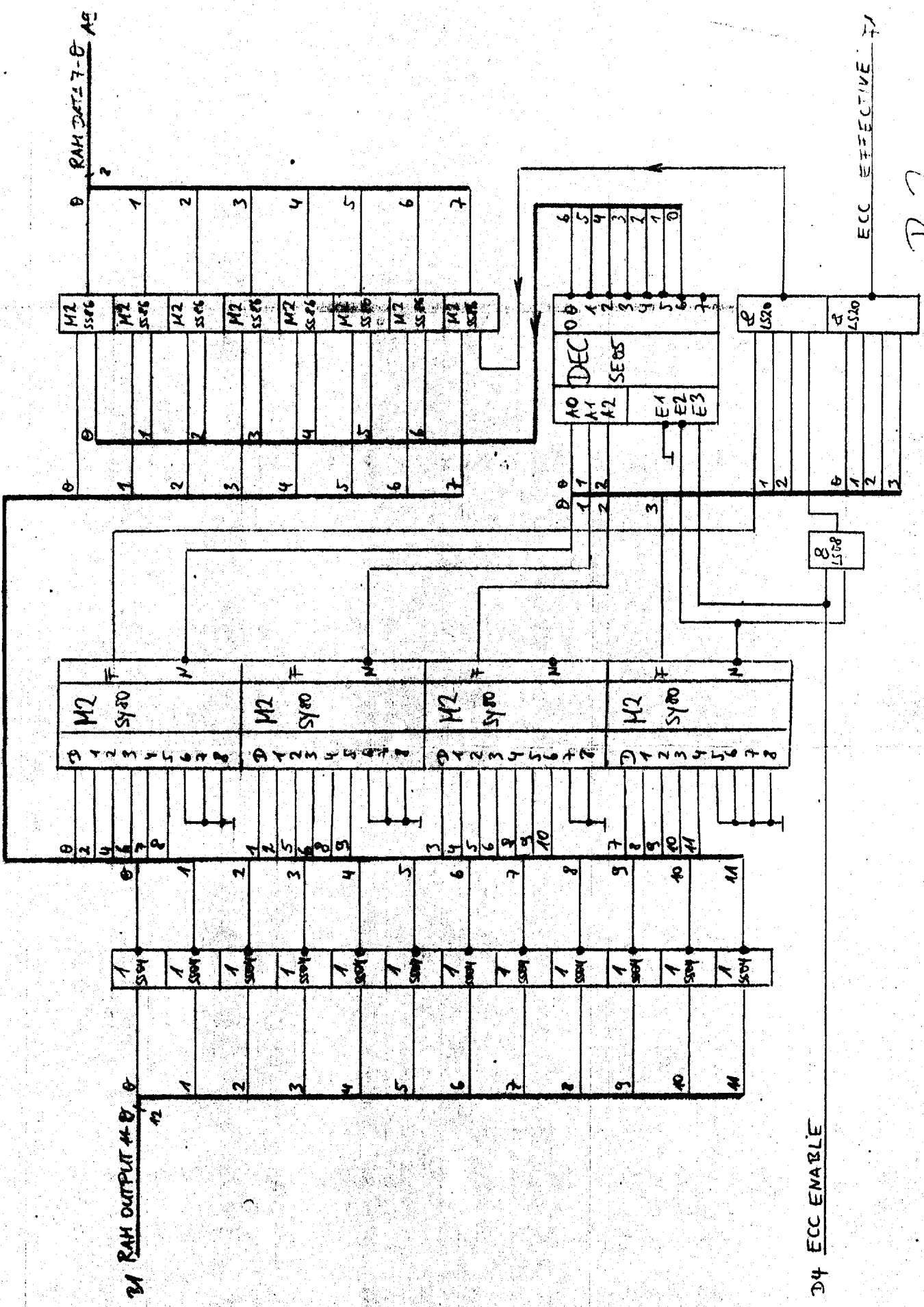
A12 RAM ADDR 7-0
 H3 /RAS
 H3 /CAS
 H3 /ECC WP
 H3 /DATA WP

A7 RAM DI 11-0



RAM OUTPUT 11-0
 M-2: 12
 2: 21

BA

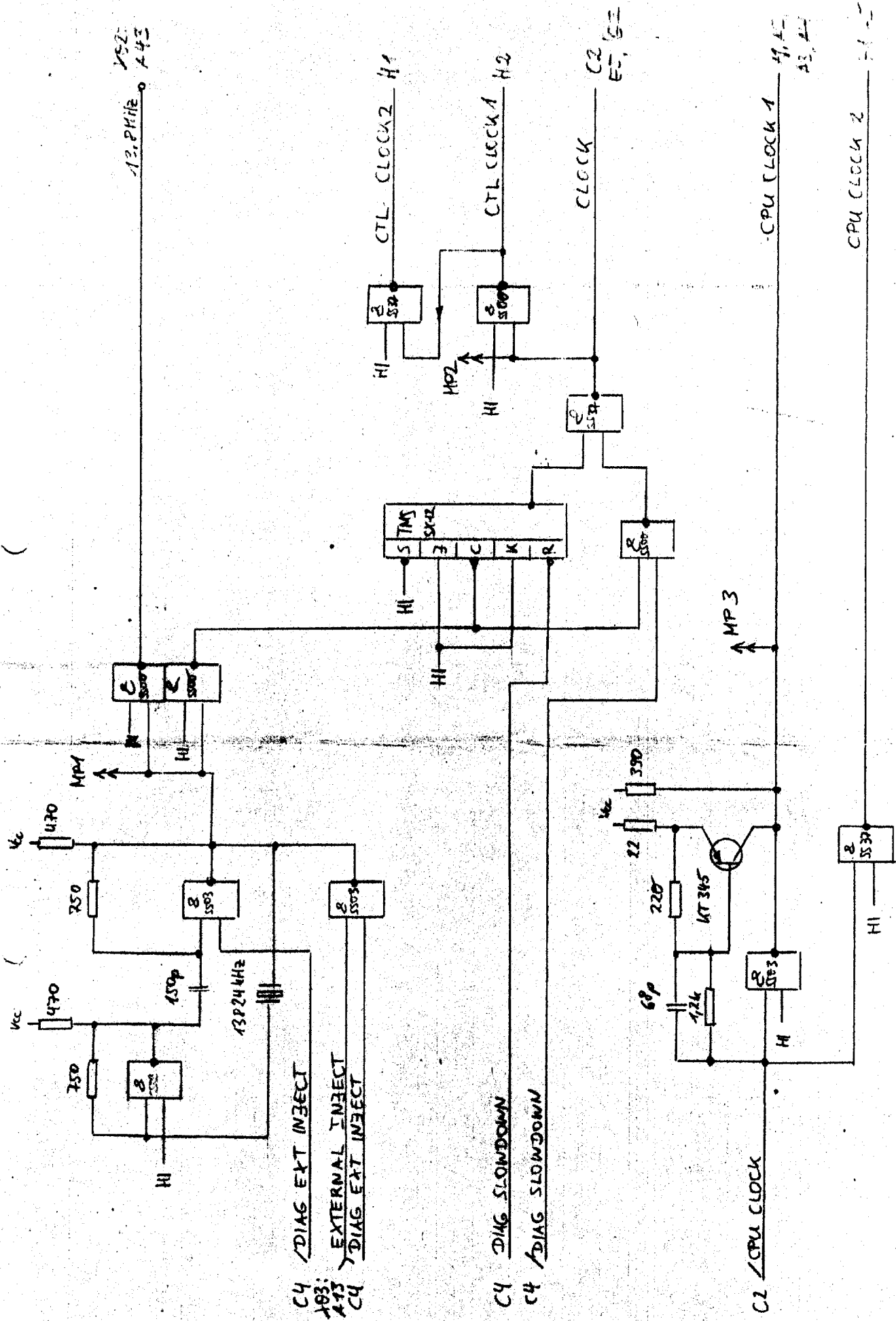


B2

RAM DATA 7-0

RAM OUTPUT 4-0

ECC EFFECTIVE



13.2MHz

CTL CLOCK 2 H1

CTL CLOCK 1 H2

CLOCK

CPU CLOCK 1

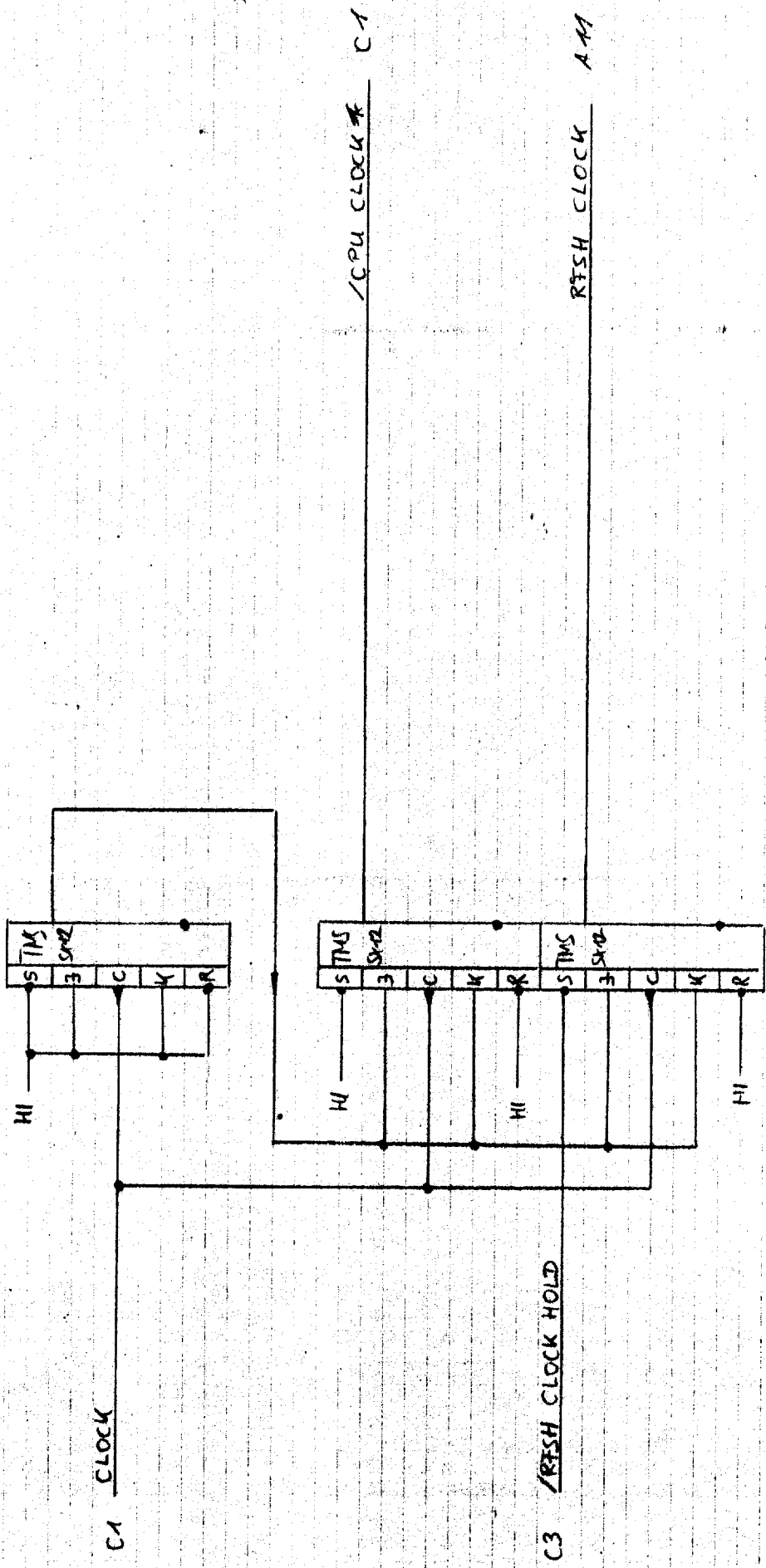
CPU CLOCK 2

C4 DIAG EXT INJECT
 X83: A43
 C4

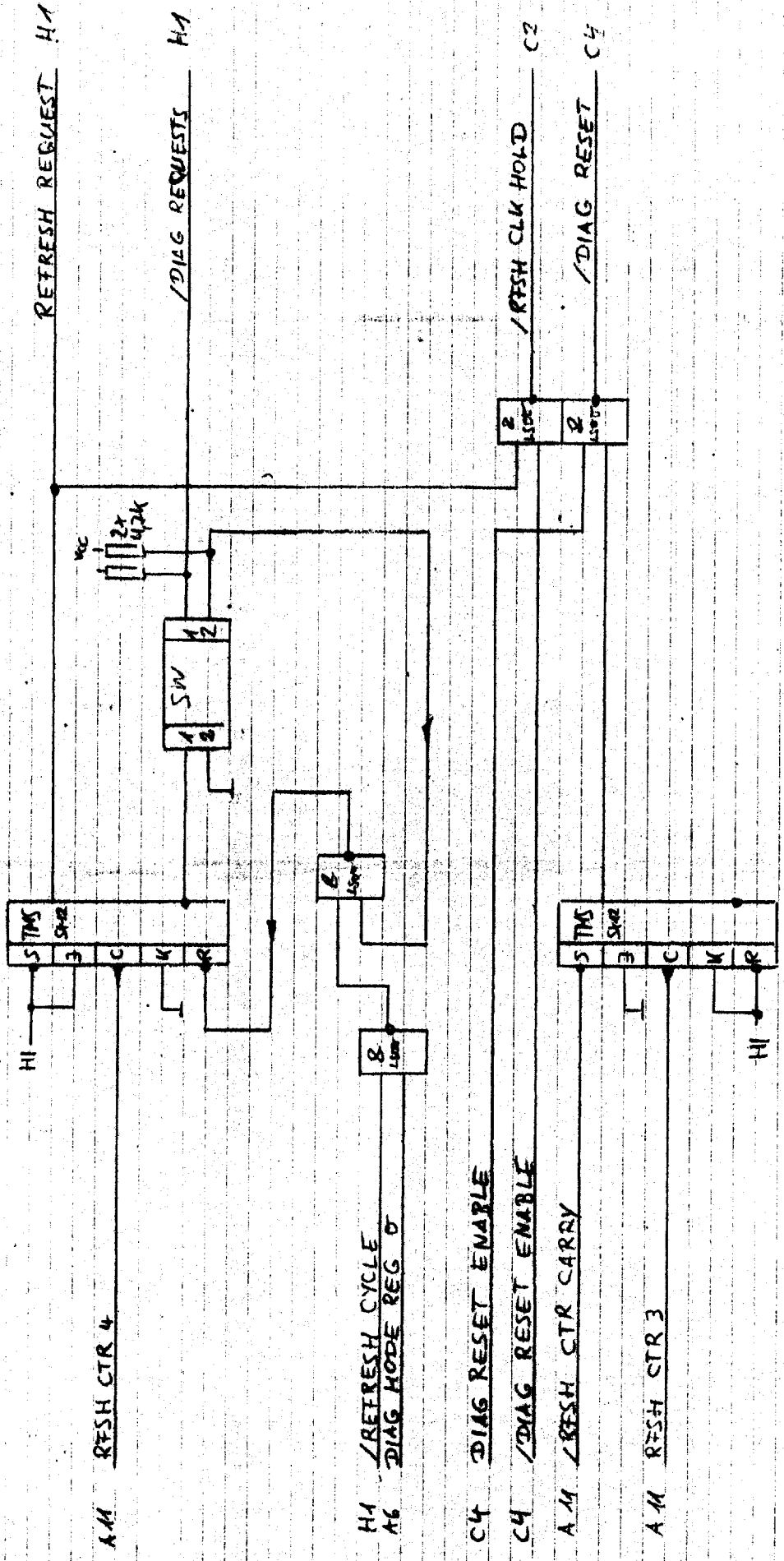
C3 DIAG SLOWDOWN
 C4 DIAG SLOWDOWN

C2 CPU CLOCK

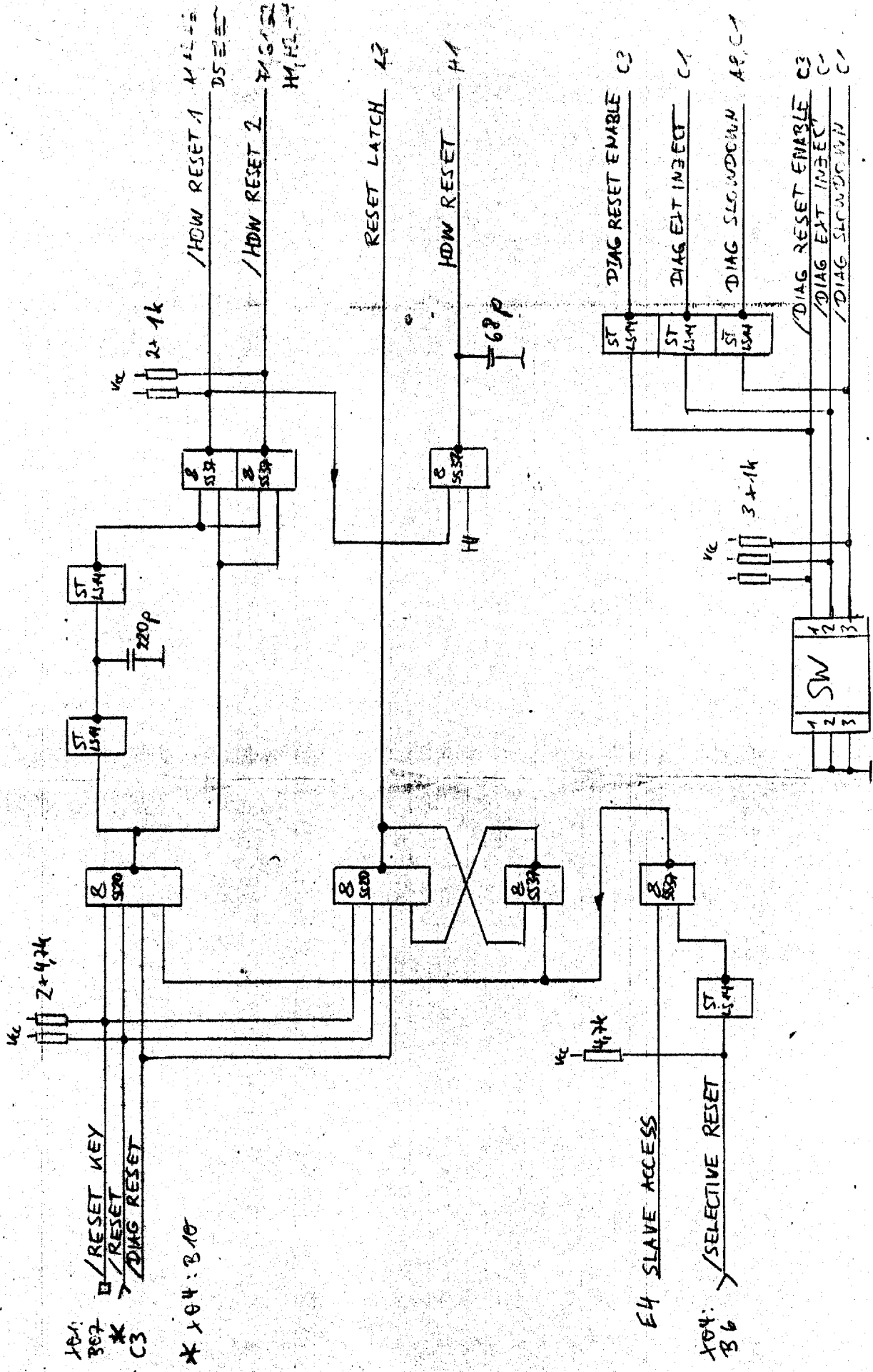
CA



C2



03



104: 302
* C3

* 104: B10

104: B6

C4

A1 CPU ADRS 15-M; 2-5 ?
 A2 /ENABLE CTC
 A3 /ENABLE SIO
 A4 /ENABLE DIO 1
 A5 /ENABLE DIO 2
 A6 /ENABLE DIO 3

A7 /MREQ
 A8 /RD
 A9 /REGISTER I/O
 A10 /ROM SELECT 0
 A11 /ROM SELECT 1
 A12 /ROM SELECT 2

A13 /RSH
 A14 CONTROL REG 3
 A15 INTERNAL EC ACCESS

A16 /DIAG ZERO FORCING
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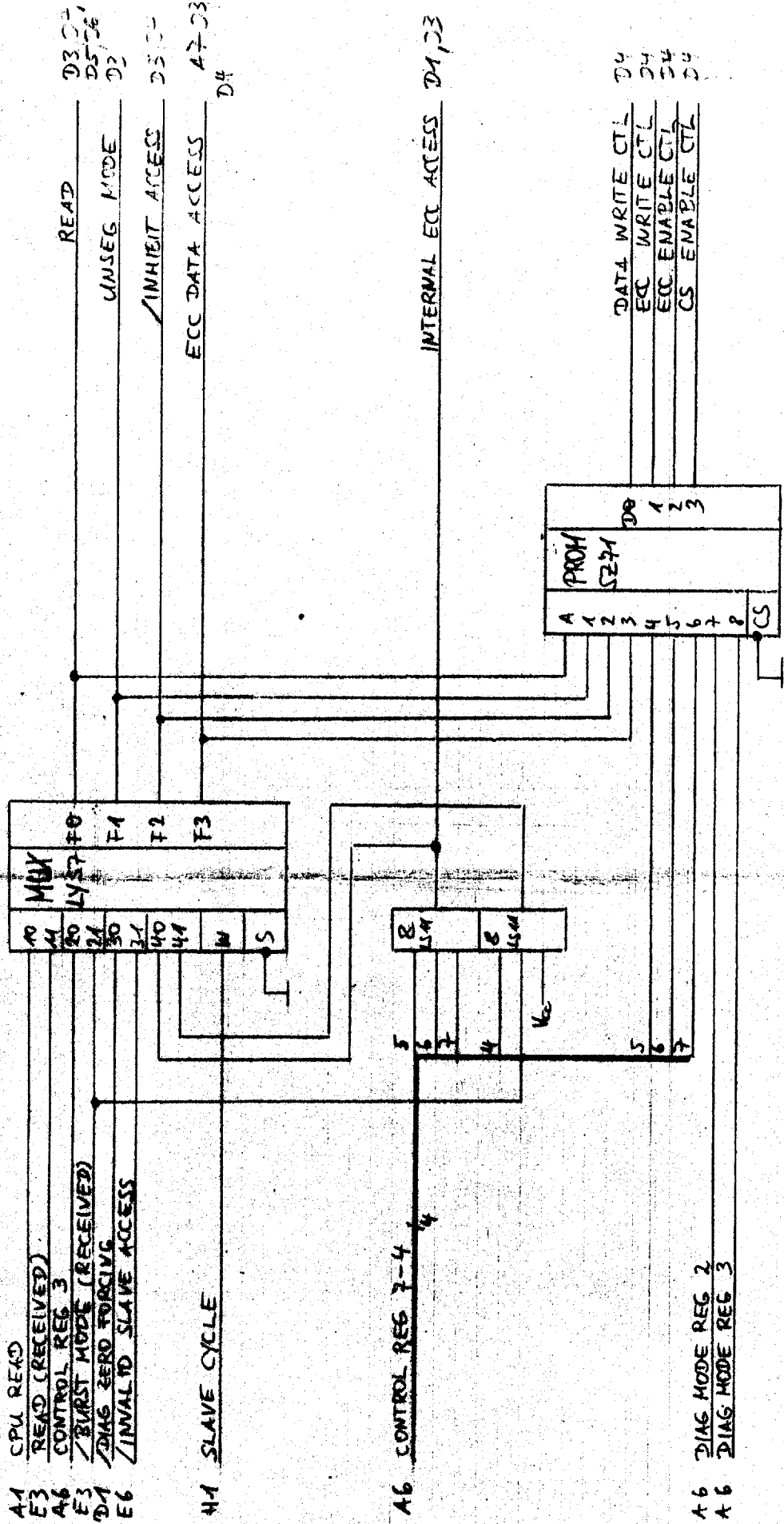
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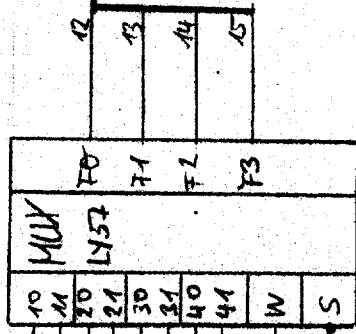
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MEU
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D2

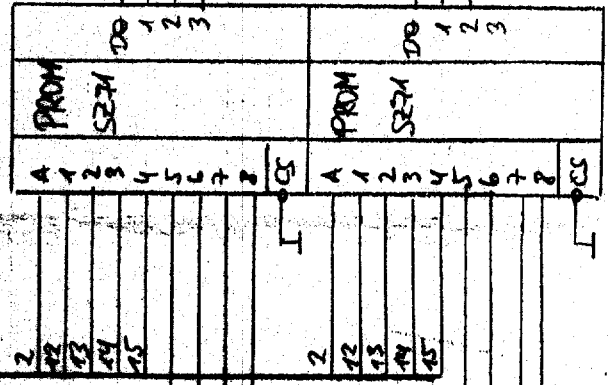
A10 COMMON ADRES 15-12:2
 A6 CONTROL REG 3-0:4



HI ADRES 12-15 A12

D2 INTERNAL ECC ACCESS

H1 /SLAVE CYCLE

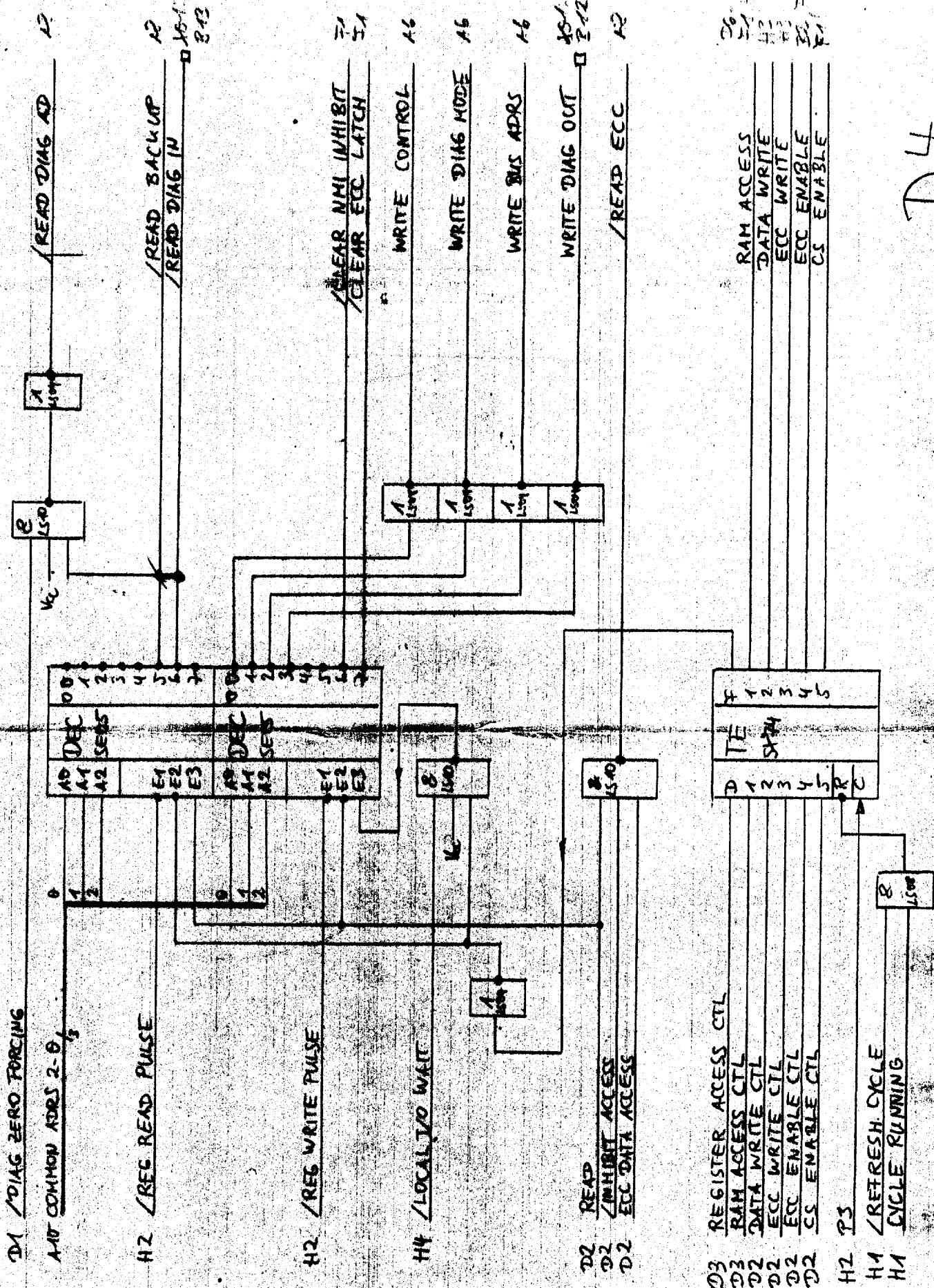


SPECIAL READ A9

REGISTER ACCESS CTL 04
 RAM ACCESS CTL 04
 ITRP STB ENABLE 06

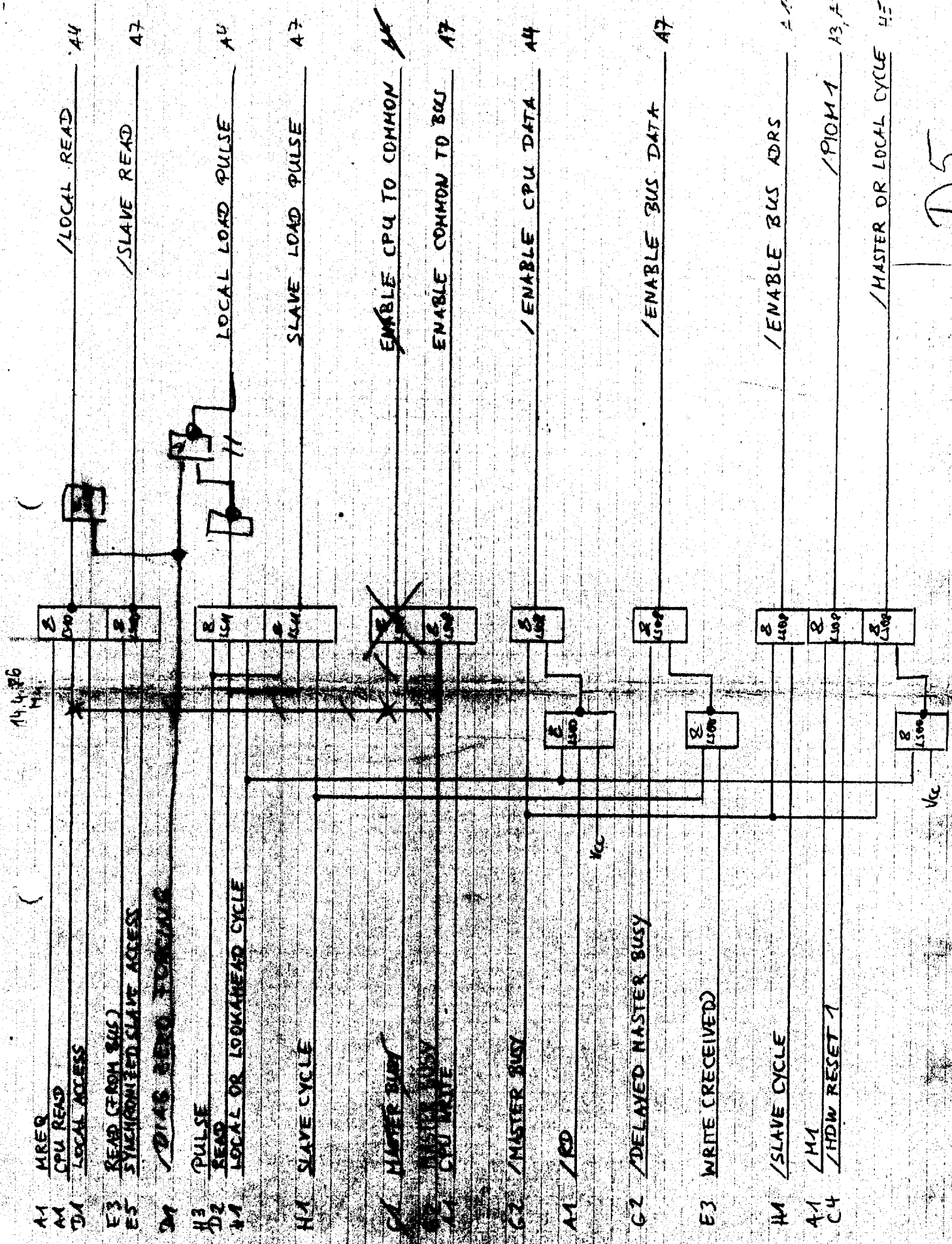
D2 READ
 D2 UNSEG MODE
 D2 /INHIBIT ACCESS
 D2 ECC DATA ACCESS

D3



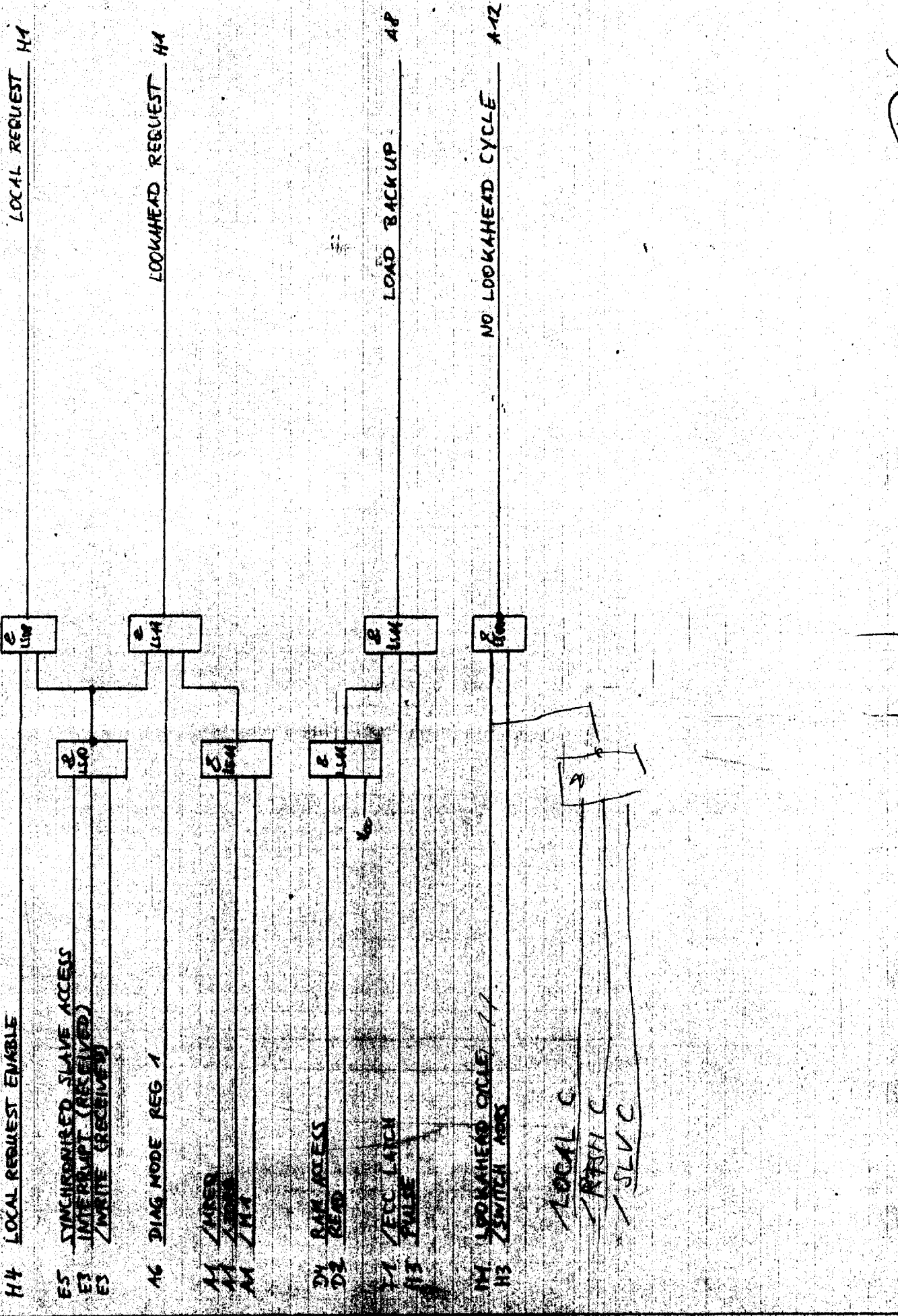
- D1 /DIAG ZERO FORCING
- A10 COMMON ADRS 2-0
- H2 /REG READ PULSE
- H2 /REG WRITE PULSE
- H4 /LOCAL TO WAIT
- D2 READ
- D2 /INHIBIT ACCESS
- D2 ECC DATA ACCESS
- D3 REGISTER ACCESS CTL
- D3 RAM ACCESS CTL
- D2 DATA WRITE CTL
- D2 ECC WRITE CTL
- D2 ECC ENABLE CTL
- D2 CS ENABLE CTL
- H2 P3
- H4 /REFRESH CYCLE
- H1 CYCLE RUNNING
- RAM ACCESS
- DATA WRITE
- ECC WRITE
- ECC ENABLE
- CS ENABLE

D4

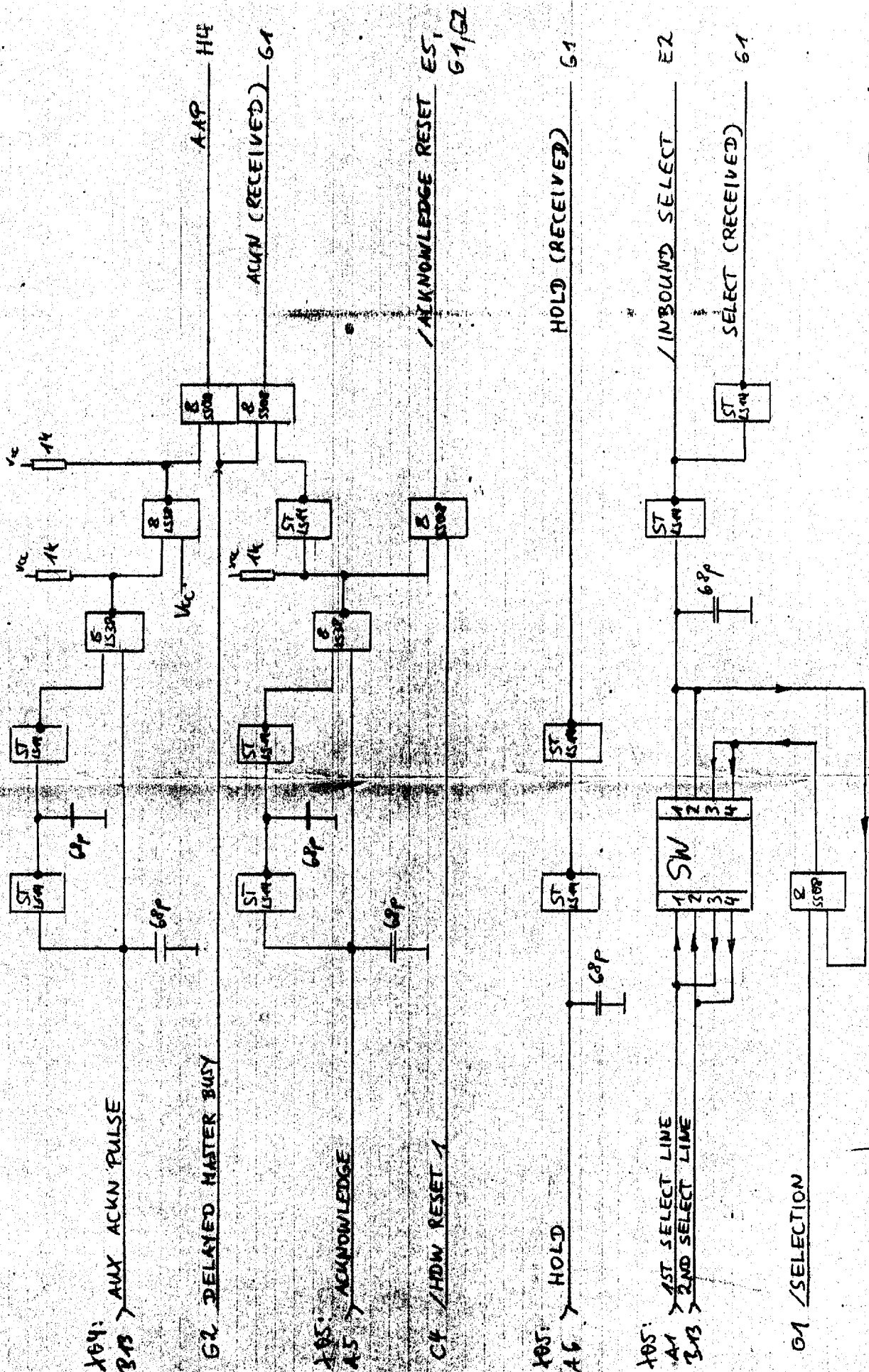


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D5



D6



E1

X05: /BUSY
A2

BUSY (RECEIVED) E4

G1 MASTER SELECTED
E1 /INBOUND SELECT

X05:

A4 /REPLY

REPLY (RECEIVED) H4

E6 LATCHED REPLY

X05:

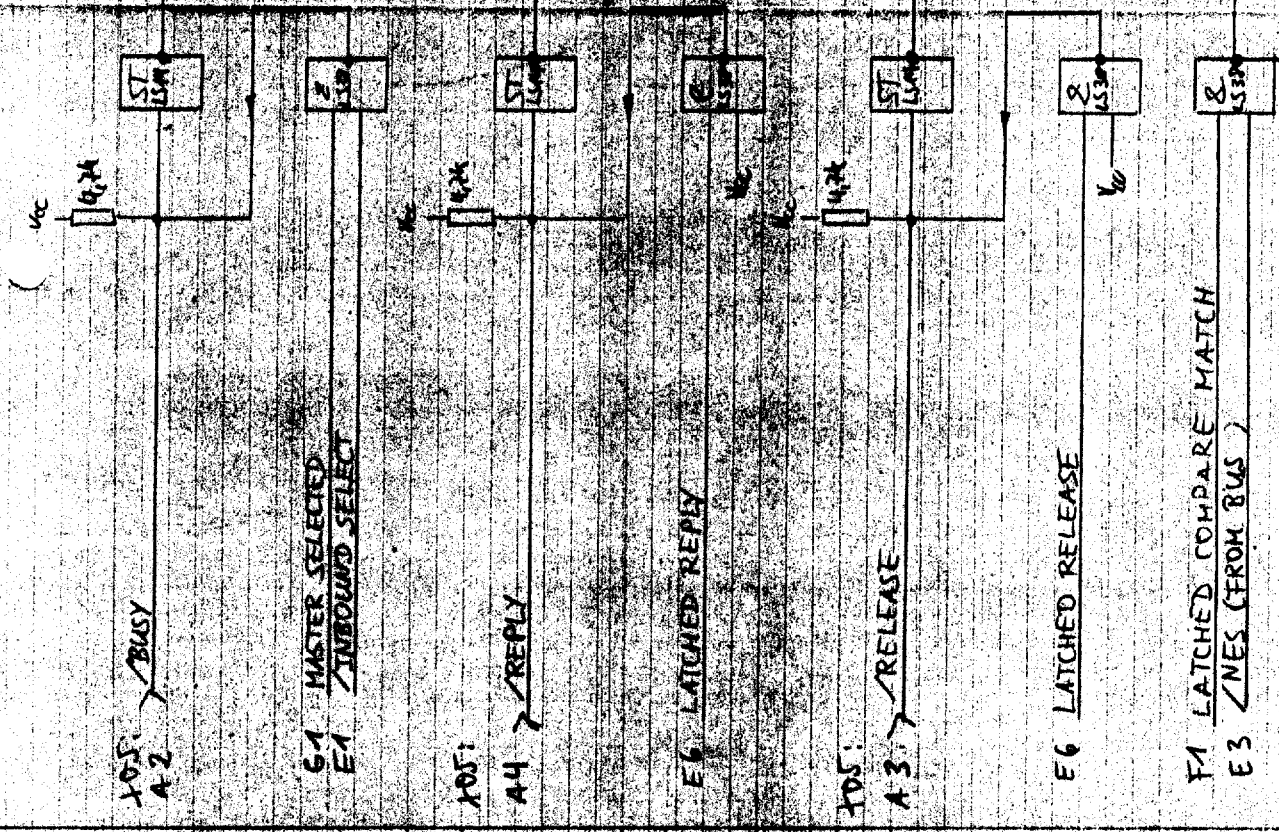
A3 /RELEASE

RELEASE (RECEIVED) G2

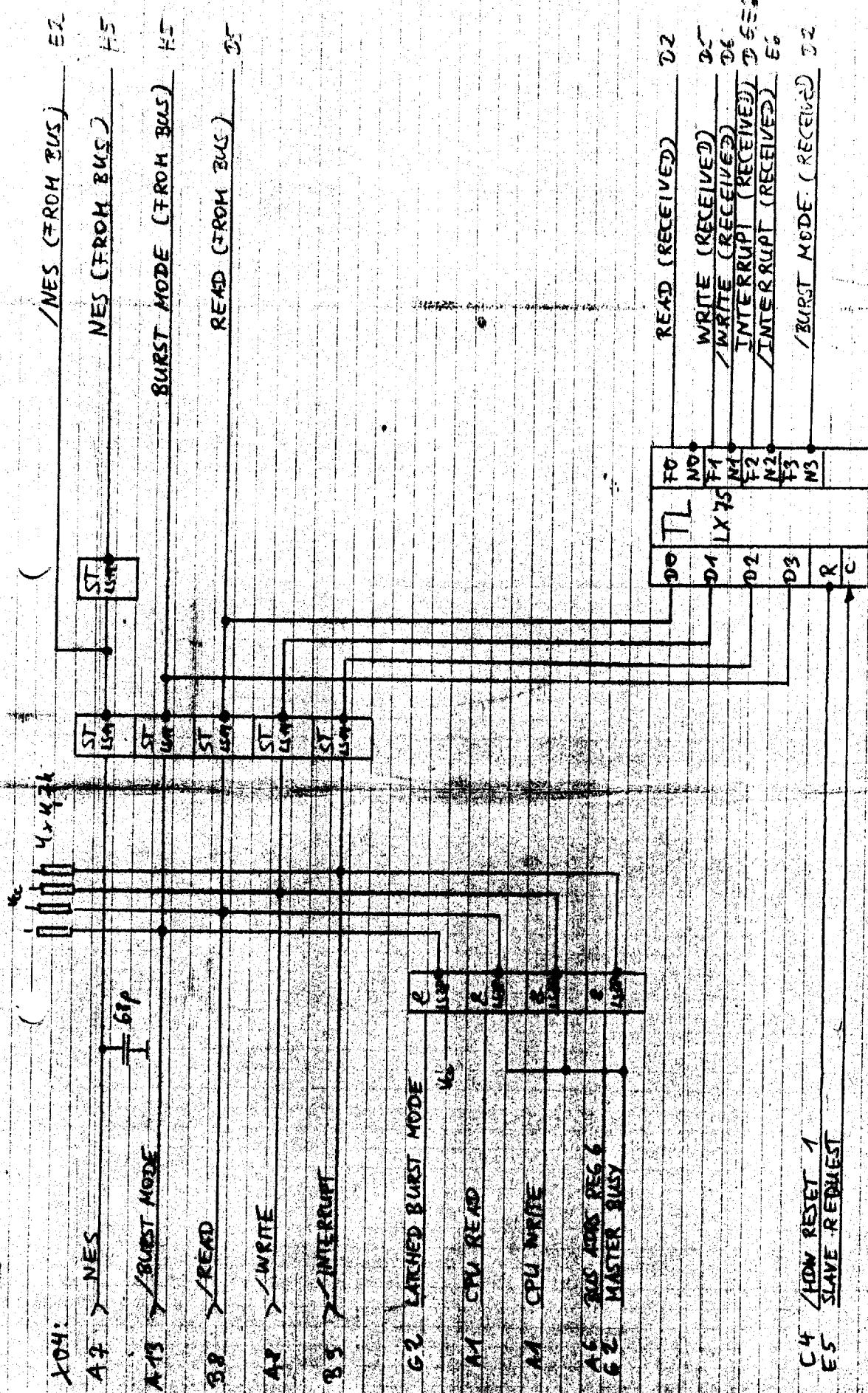
E6 LATCHED RELEASE

F1 LATCHED COMPARE MATCH
E3 /NES (FROM BUS)

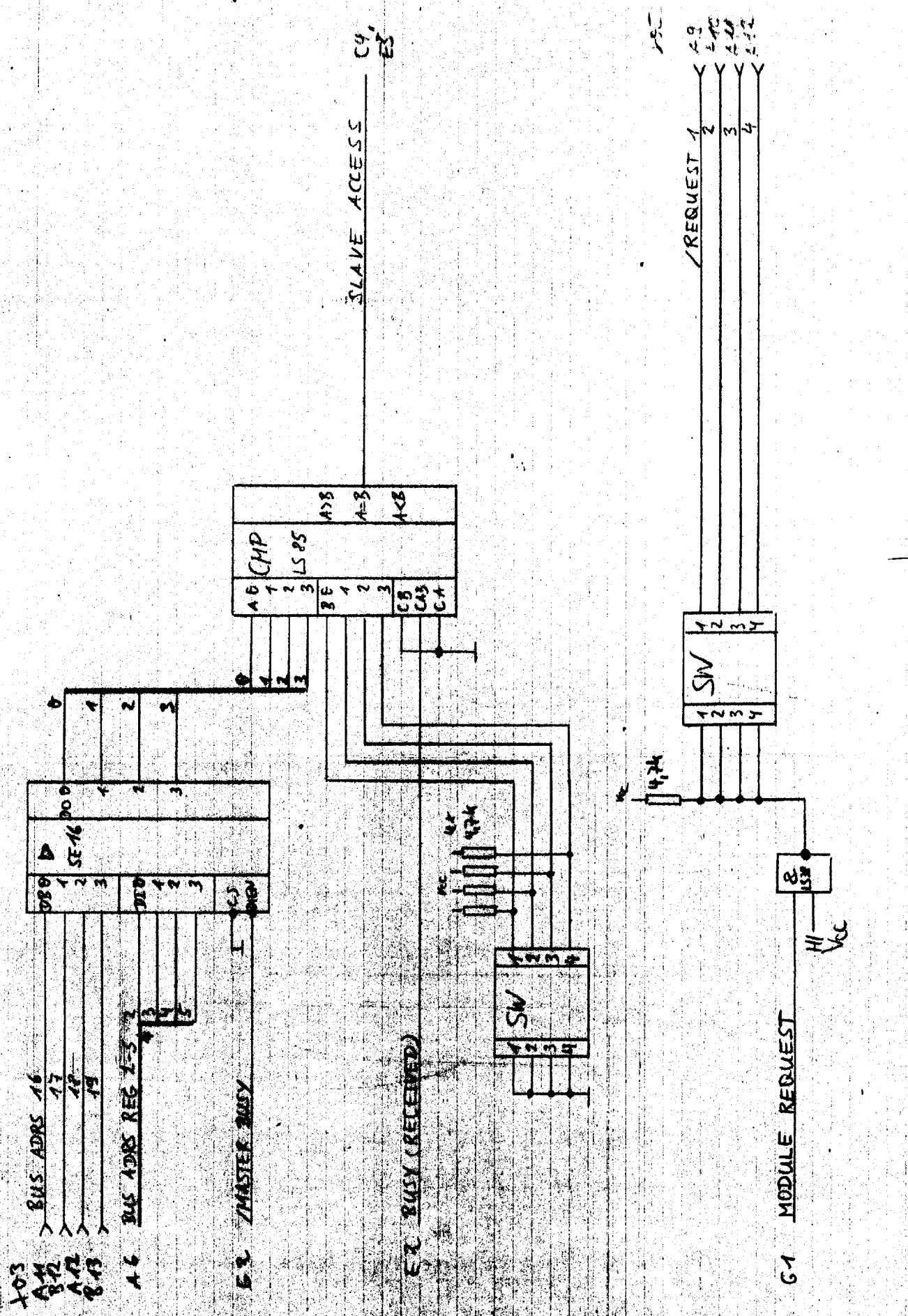
X04: /COMPARE MATCH
B4



E2



E3



E7
E4

E4 SLAVE ACCESS



SYNCHRONIZED SLAVE ACCESS



E6, E7

C1 - CLOCK

E1 / ACKNOWLEDGE RESET



SLAVE REQUEST

E4

C4 / HDW. RESET 1
H1 / SLAVE CYCLE

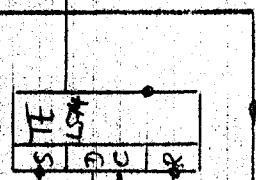
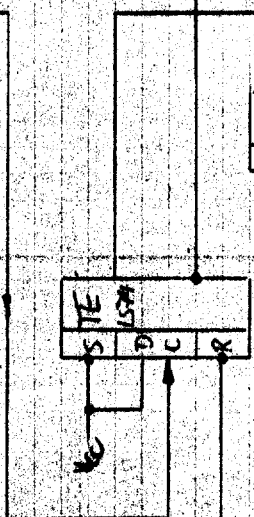
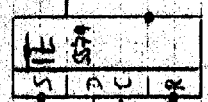
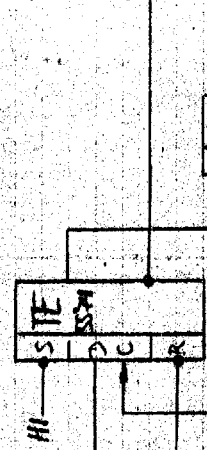


H2 P3
H2 / END

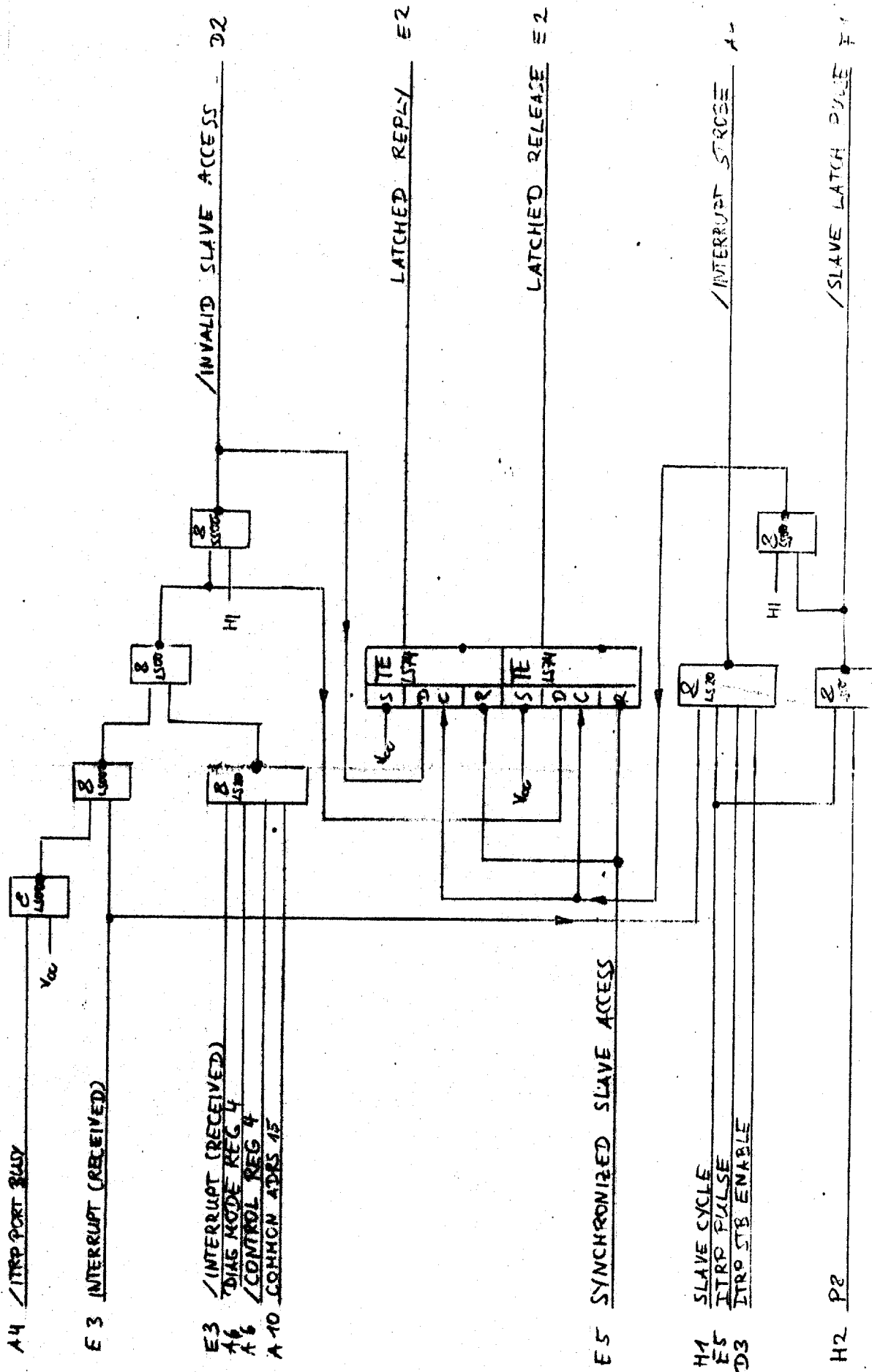


ITRP PULSE

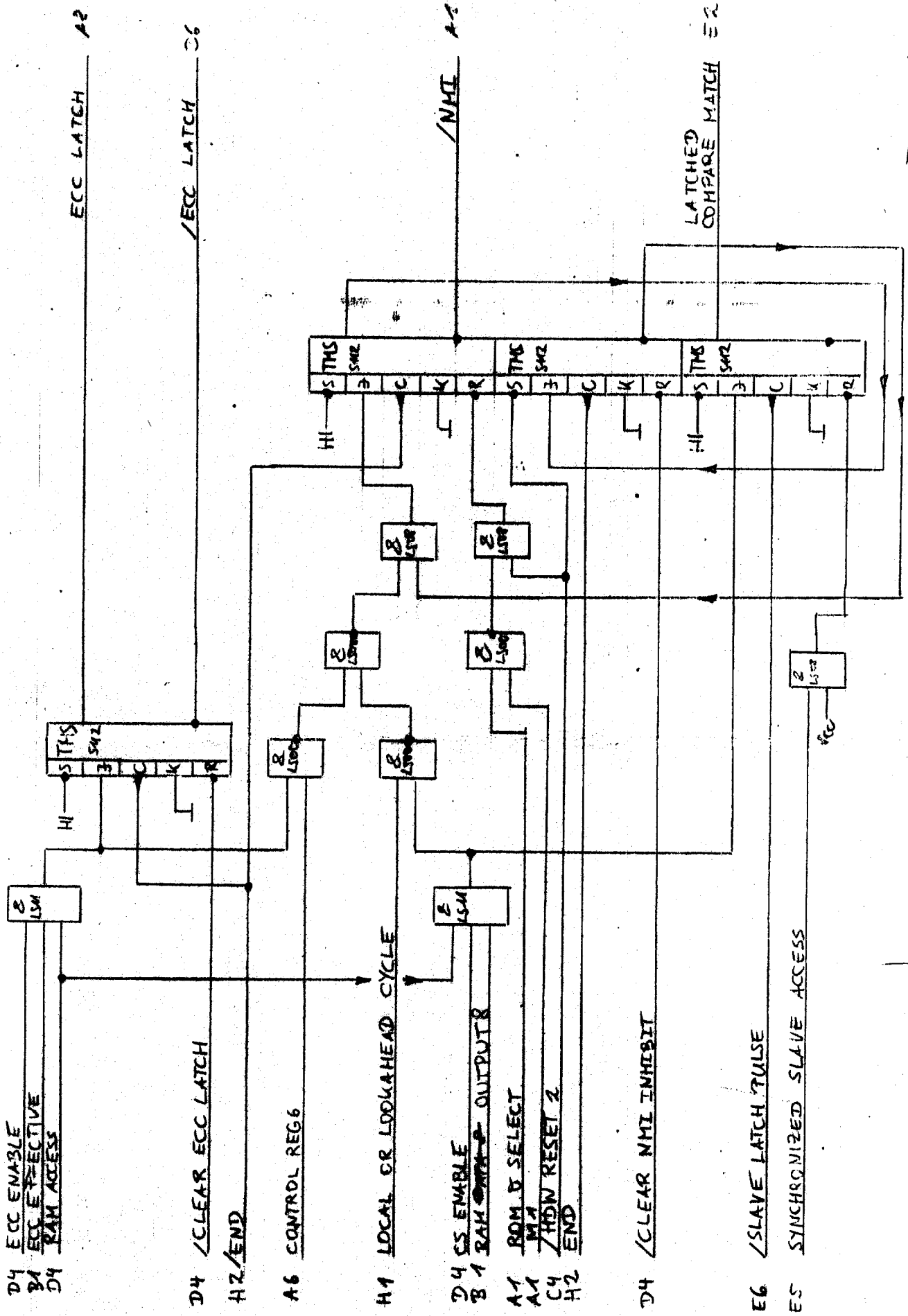
E6



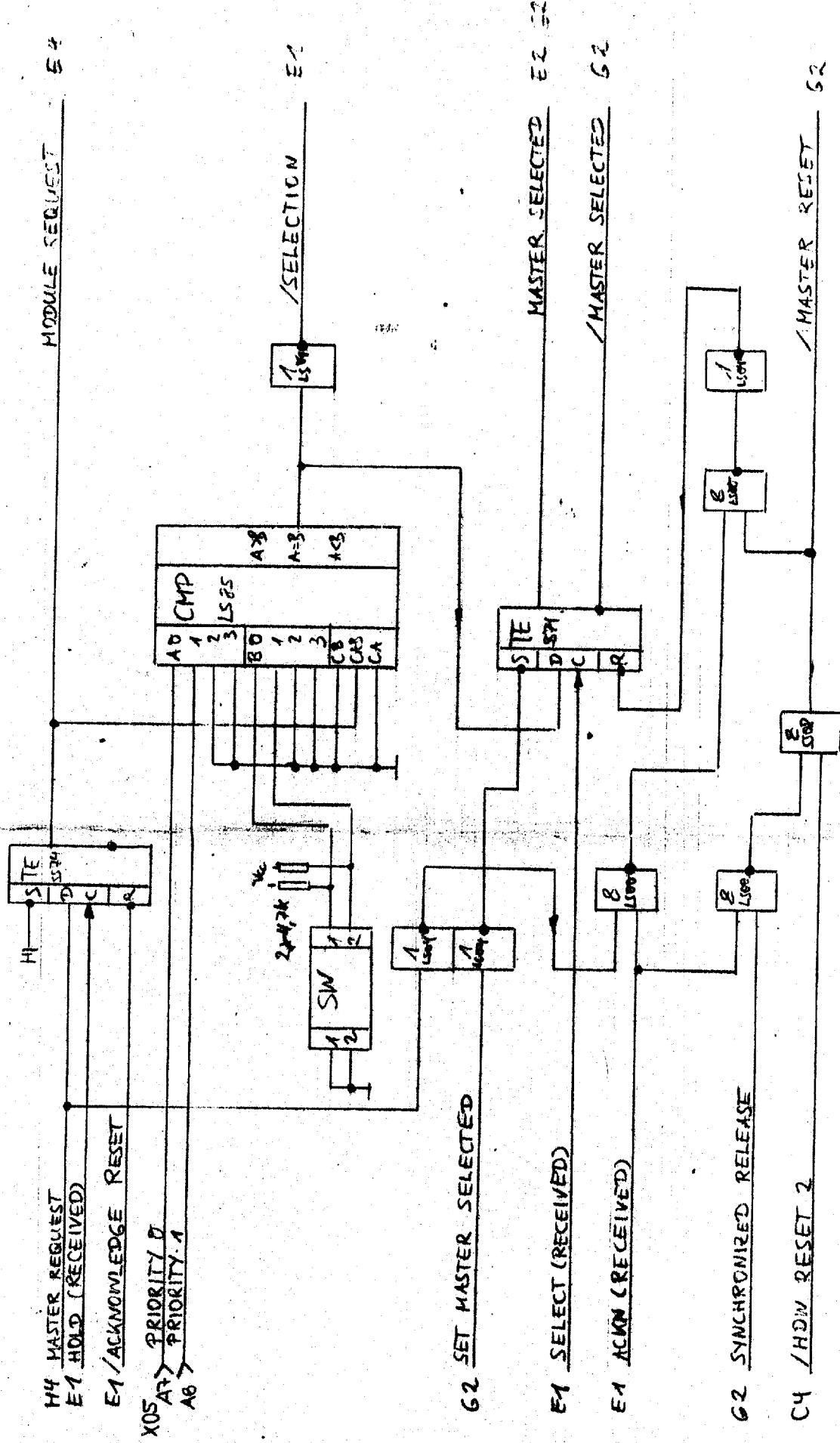
E5



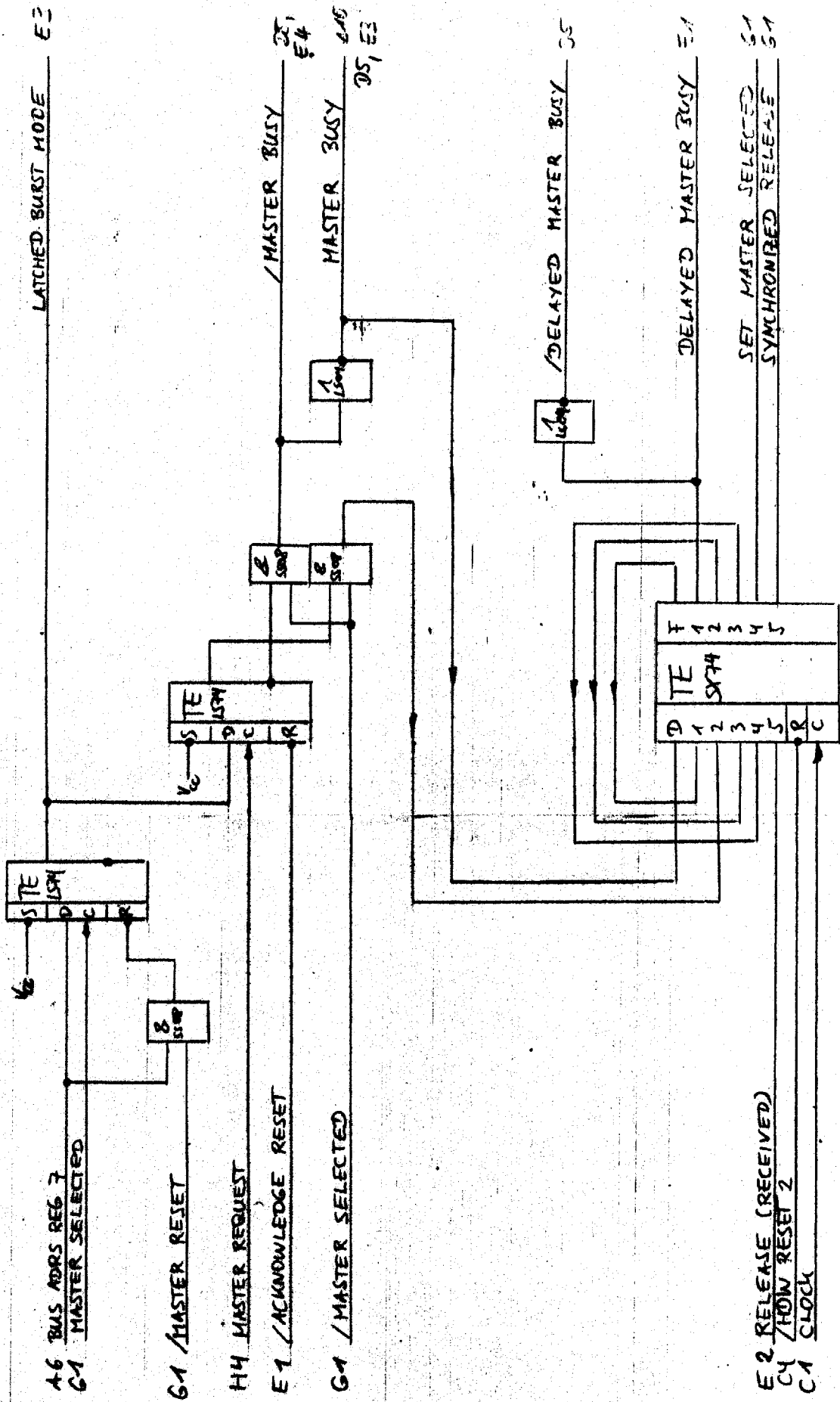
E6



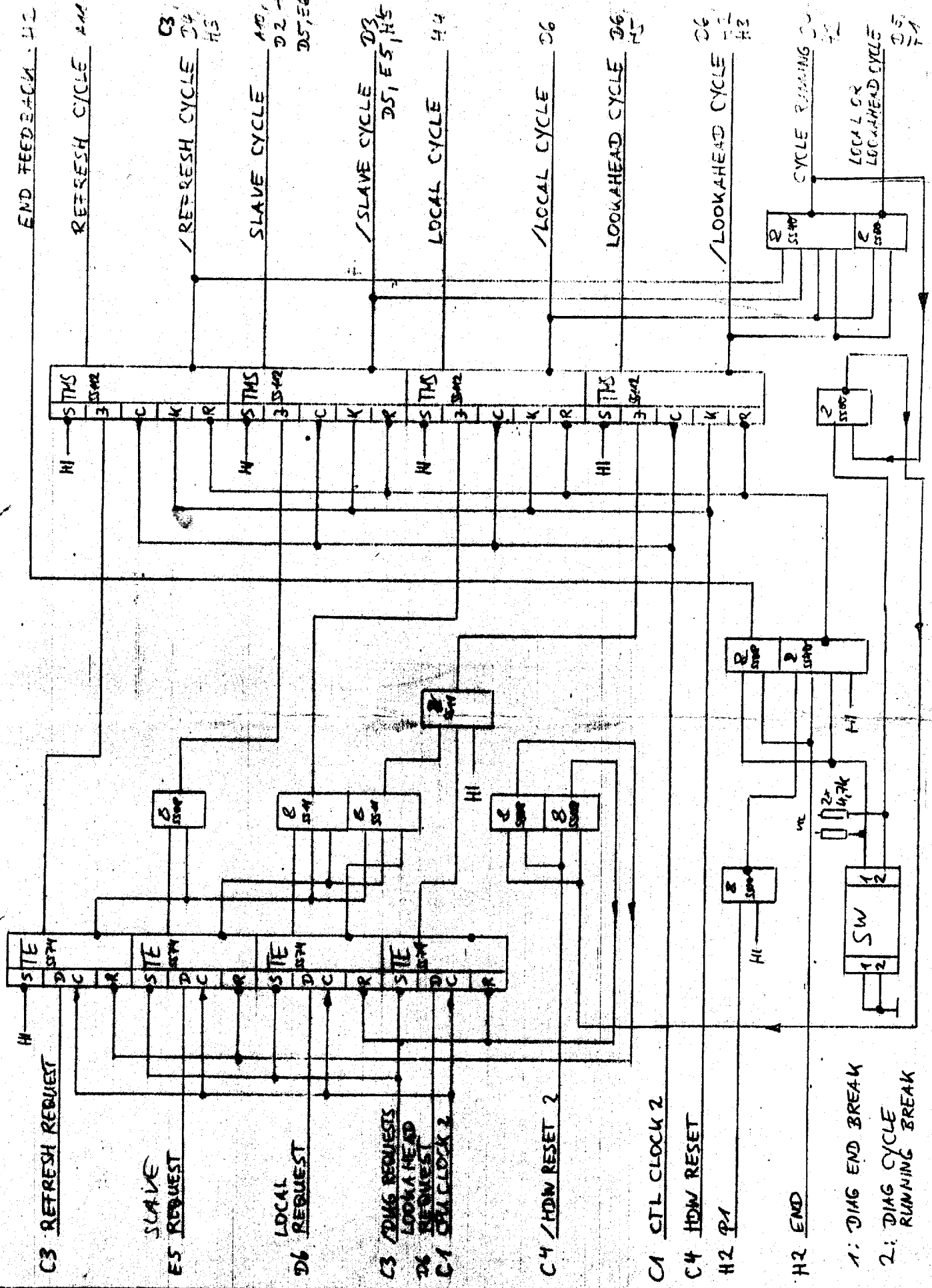
EM



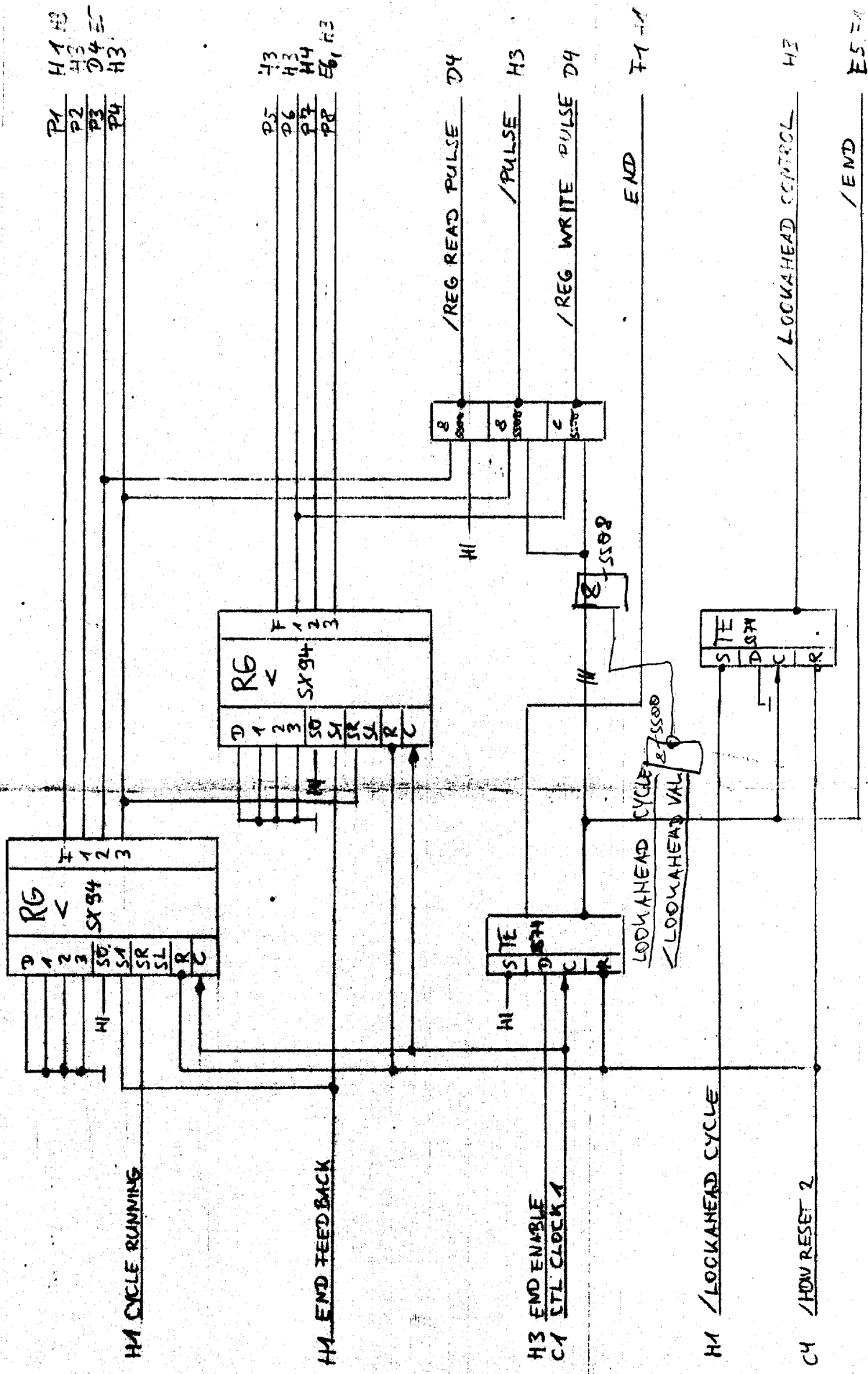
G1



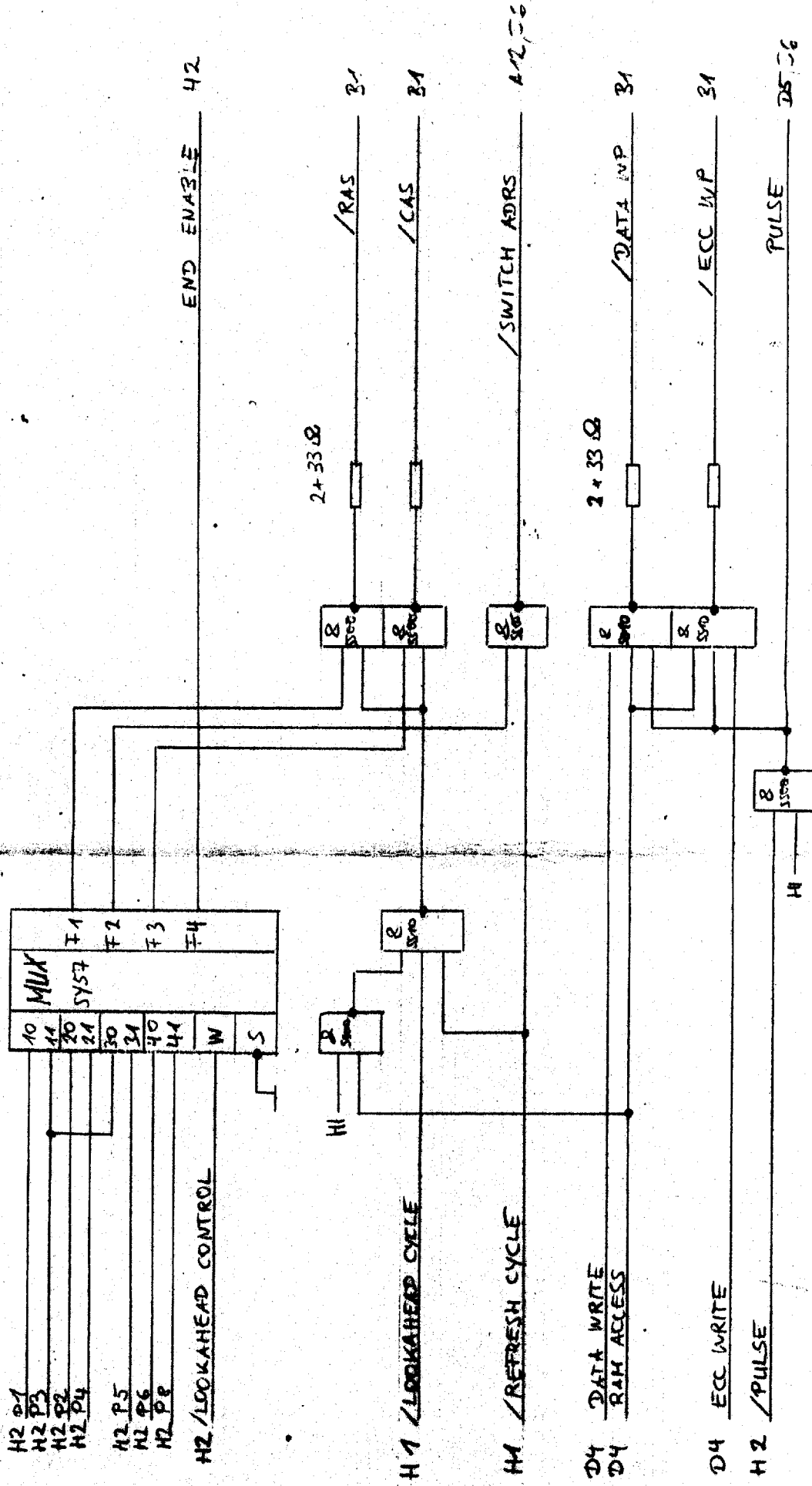
62

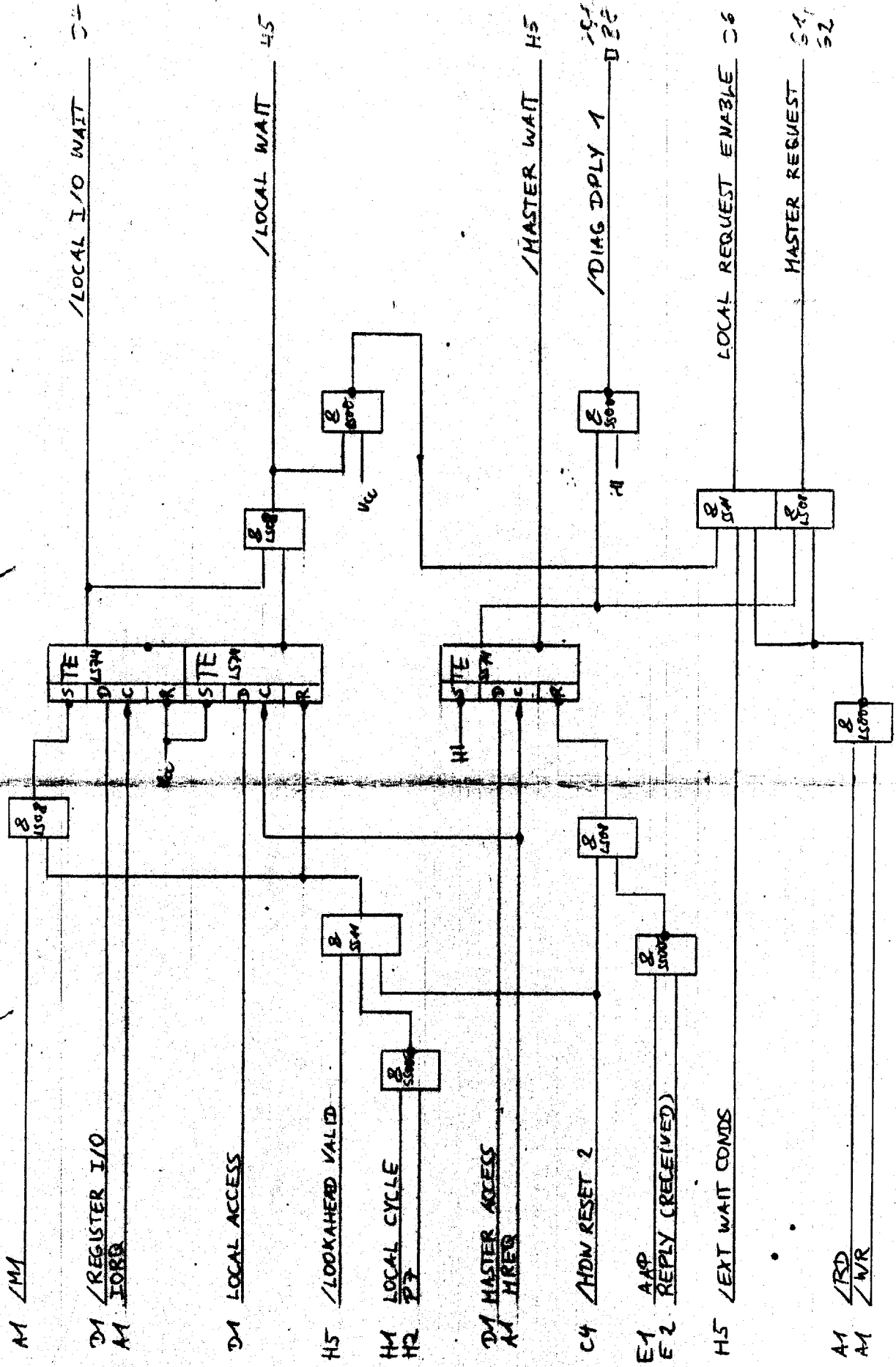


H1

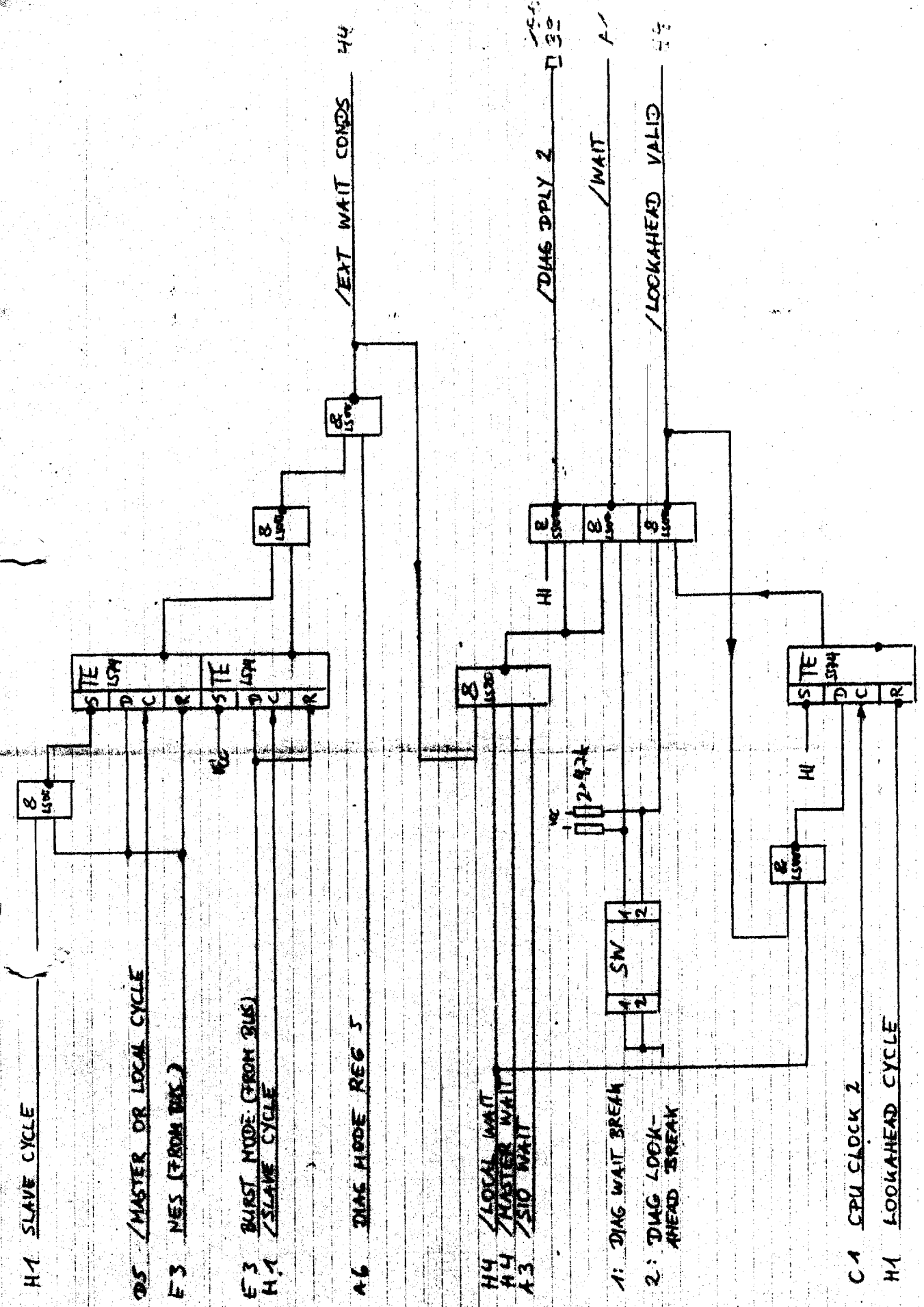


H12





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H1 SLAVE CYCLE
 05 MASTER OR LOCAL CYCLE
 E3 NES (FROM BUS)
 E3 BURST MODE (FROM BUS)
 H1 SLAVE CYCLE
 A6 DIAG AHDE REG 5
 H4 LOCAL WAIT
 H4 MASTER WAIT
 A3 SIO WAIT
 1: DIAG WAIT BREAK
 2: DIAG LOOK-AHEAD BREAK
 C1 CPU CLOCK 2
 H1 LOOKAHEAD CYCLE

H5