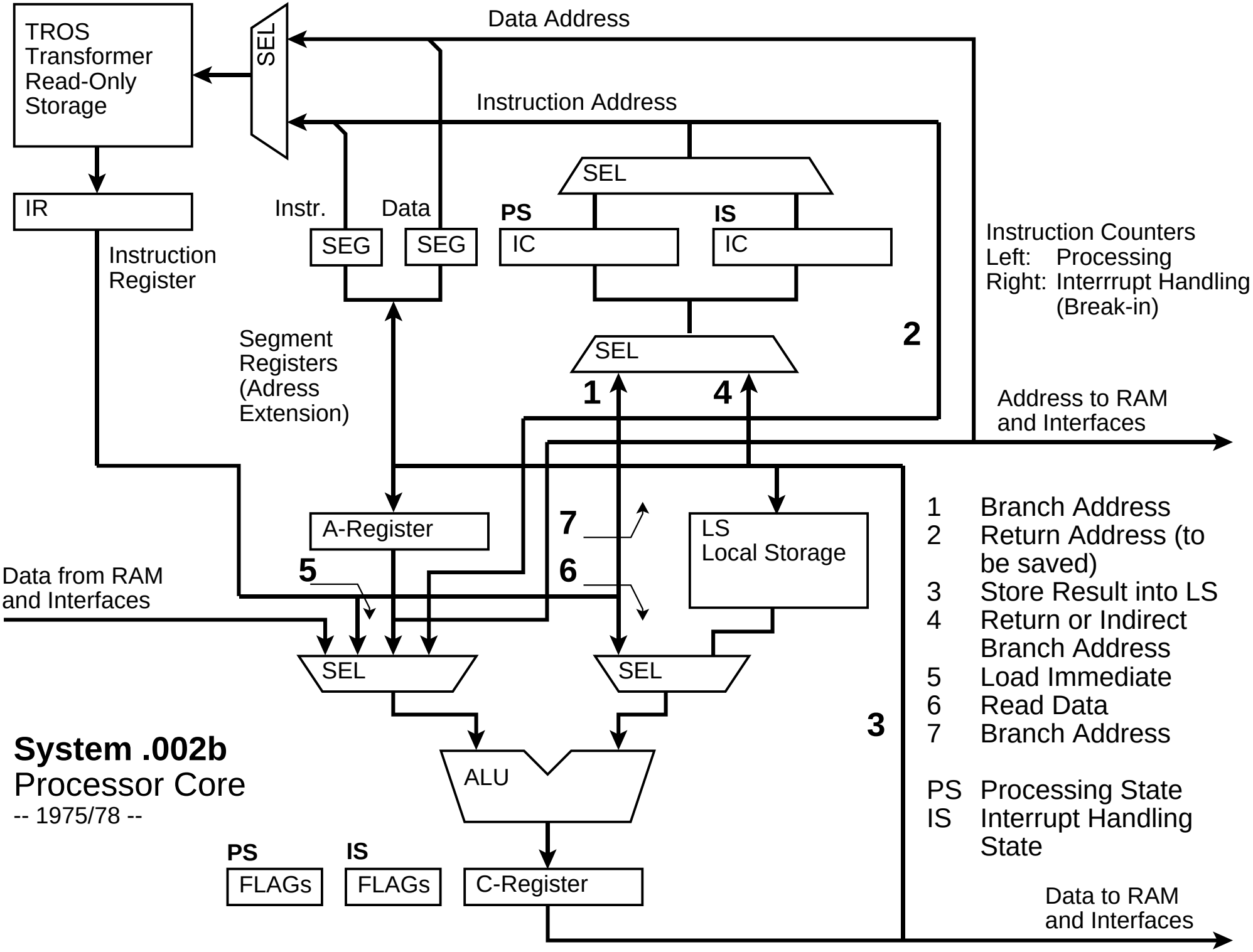
TROS
Transformer
Read-Only
Storage
SEL
Data Address
Instruction Address
IR
Instr.
Data
SEG
SEG
PS
IS
SEL
IC
IC
Instruction
Register
Instruction Counters
Left: Processing
Right: Interrrupt Handling
(Break-in)
Segment
Registers
(Adress
Extension)
SEL
2
1
4
Address to RAM
and Interfaces
A-Register
7
LS
Local Storage
5
6
Data from RAM
and Interfaces
SEL
SEL
3
ALU
PS
IS
FLAGs
FLAGs
C-Register
Data to RAM
and Interfaces
1 Branch Address
2 Return Address (to be saved)
3 Store Result into LS
4 Return or Indirect Branch Address
5 Load Immediate
6 Read Data
7 Branch Address
PS Processing State
IS Interrupt Handling State
System .002b
Processor Core
-- 1975/78 --