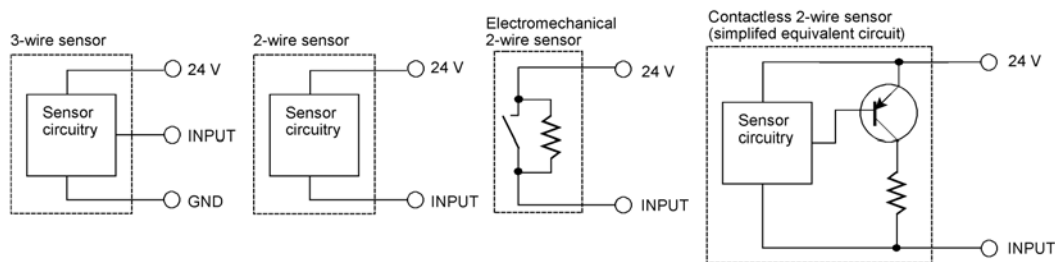


## Voltage-level translation in MCU projects – Addendum –

### 3-wire and 2-wire sensors

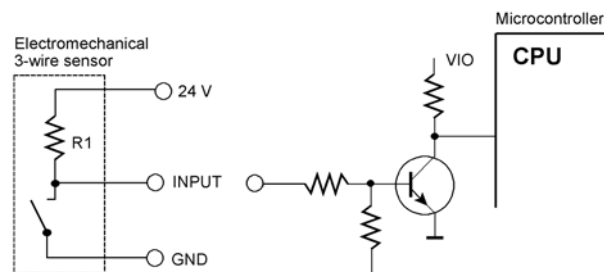
The 3-wire sensor is easy to understand. It is a device powered by a 24-V supply voltage and energizing a digital output signal to be connected to an input of the level-translating circuitry. A 2-wire sensor is only connected to a 24-V wire and the signal wire. To power such a sensor, some current must always flow.



**Figure A1** 3-wire and 2-wire sensors.

### Simple and IEC-compliant 24-V inputs

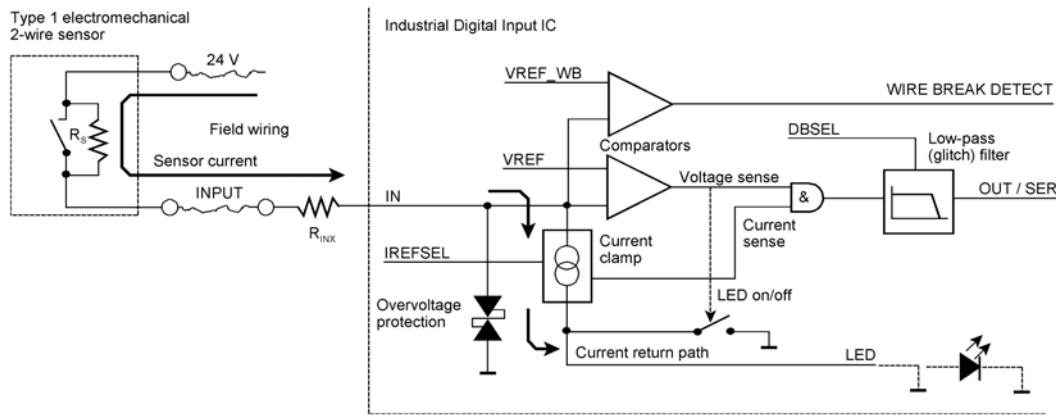
A simple input senses only the voltage level. Contact sensors (e.g., limit switches) are the most straightforward examples.



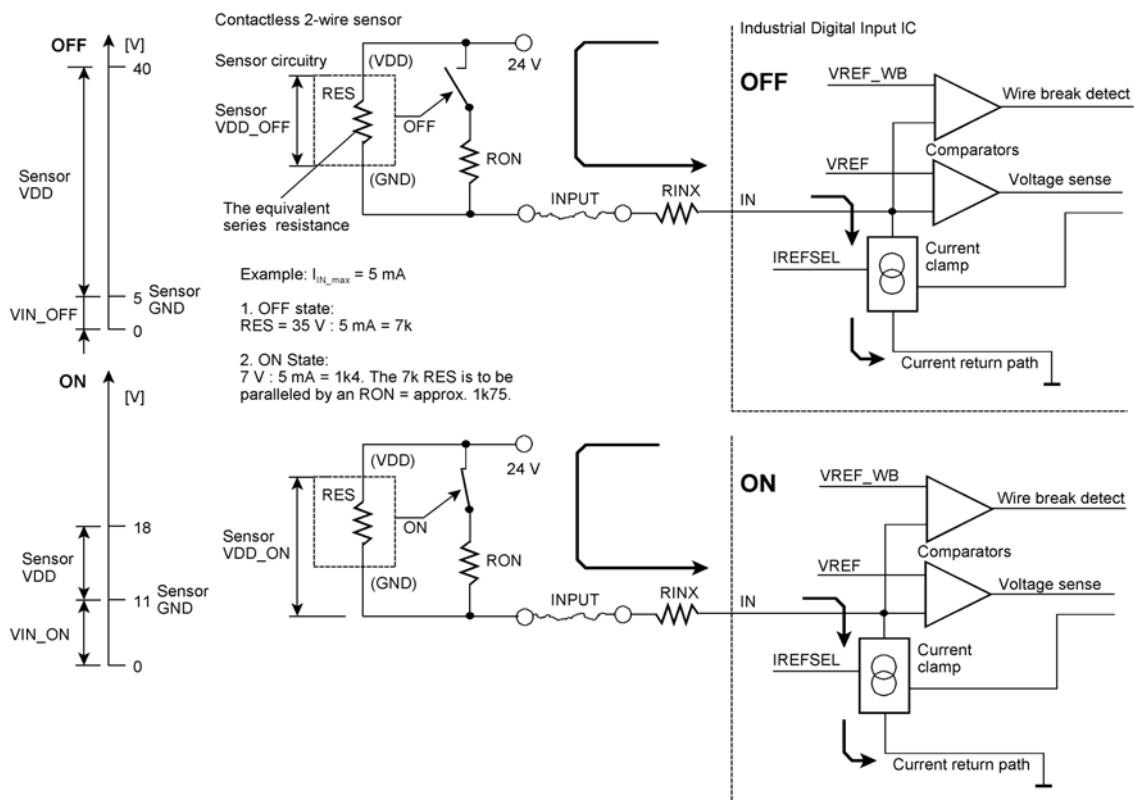
**Figure A2** This 3-wire sensor switches the input signal between 24 V (or somewhat below due to the voltage drop over R1) and 0 V. Only the signal level is to be translated. It can be done by a few discrete components.

An IEC-compliant sensor, however, always behaves as a current source. Current flows from the 24-V terminal through the sensor and the signal wire and the input circuitry of the translating device to ground.

How to power the circuitry in a contactless 2-wire sensor (e.g., in a proximity switch)? Power is supplied by letting a current flow from the 24-V terminal via the input wire to ground. Therefore, the translation circuitry must behave as a current sink. In the OFF state, the signal must not rise above 5 V. In the ON state, it must be at 11 V or above. According to the IEC type, a current of up to 15 or even 30 mA may flow through the sensor.



**Figure A3** Here, some internals of the MAX22190 Octal Industrial Digital Input IC are shown ([22]). The circuitry resembles Figure 14 in the printed article. However, it is supplemented by provisions to detect a broken wire or a short to ground. The sensor must source some current, even if in the OFF state. Hence the contact is paralleled by a resistor  $R_S$ , ensuring a minimum current flow. So, no current at all will indicate a wire break fault condition.



**Figure A4** Powering a 2-wire sensor. The sensor's circuitry may be seen as an equivalent series resistance causing a voltage drop because of the flowing current. This is the sensor's supply voltage (VDD).

### A simple worst-case analysis

It will be something like a calculation on the back of an envelope. Let us assume a 24-V supply voltage varying between 18 and 40 V and a current limit of 5 mA. To make things not too

complicated, we will furthermore neglect the input series resistors  $R_{INX}$  (that are mandatory for these ICs).

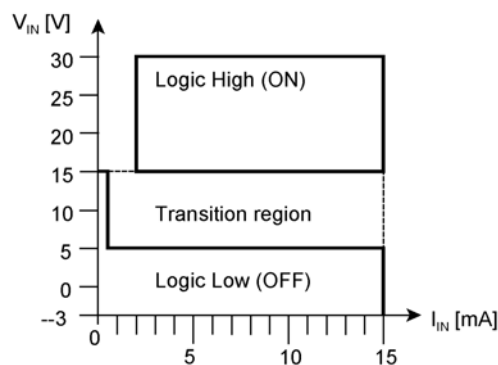
In the OFF state, the current flows only through the equivalent series resistance  $R_{ES}$ . The voltage drop must be large enough so that the voltage at the input terminal is well below the maximum  $V_{IN\_OFF}$  ( $V_{IL}$ ) voltage of 5 V (as stipulated in IEC61131-2). The worst case occurs if the sensor is fed with 40 V. Thus the voltage drop must become 35 V, yielding an  $R_{ES} = 35 \text{ V} : 5 \text{ mA} = 7 \text{ k}\Omega$ .

In the ON state, the sensor's circuitry will activate an additional parallel resistance  $R_P$  to decrease the voltage drop. It must be reduced so that the voltage at the input terminal is well above the minimum  $V_{IN\_ON}$  ( $V_{IH}$ ) voltage of 11 V (as stipulated in IEC61131-2). The worst case occurs if the sensor is fed with 18 V. To guarantee a voltage drop of not more than 7 V, the resistance of the sensor must be reduced to  $7 \text{ V} : 5 \text{ mA} = 1.4 \text{ k}\Omega$ . To this end, the sensor must activate a parallel Resistor  $R_P$  of approx. 1.75 k $\Omega$ .

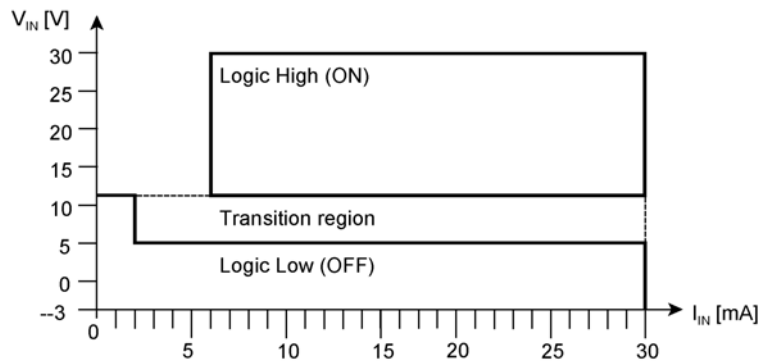
The sensor's circuitry must be content with an intensively varying power supply. In our example, the supply voltage ( $V_{DD}$ ) corresponds to the voltage drop varying between 7 and 35 V and the current may plummet down to somewhat around 2 mA.

The power requirement of the sensor and the current-sinking capability of the translation device must fit together. For example, it will not work if the current clamp within the translation IC limits the input current to 2 mA while the sensor needs 5 mA.

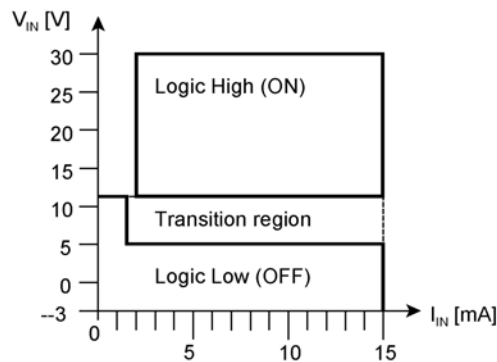
### IEC 61131-2 sensor types and operating regions



**Figure A5** IEC 61131-2 type 1 operating regions. Type 1 concerns mechanical contacts and 3-wire sensors drawing a comparatively high quiescent current.

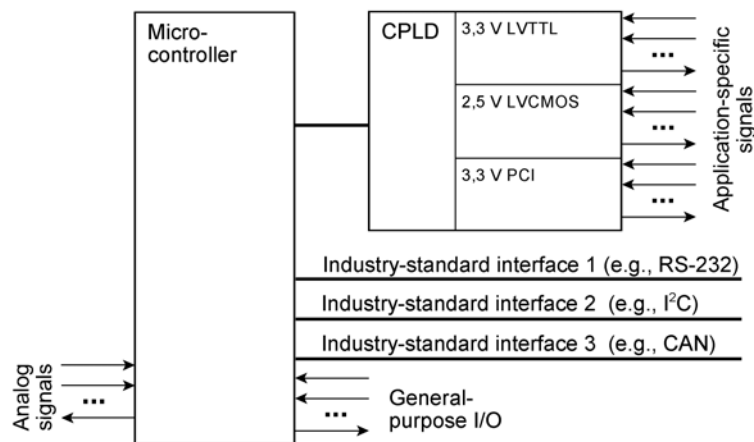


**Figure A6** IEC 61131-2 type 2 operating regions. Type 2 relates to 2-wire sensors with a somewhat increased power consumption, for example, 2-wire proximity switches according to IEC 60947-5-2.



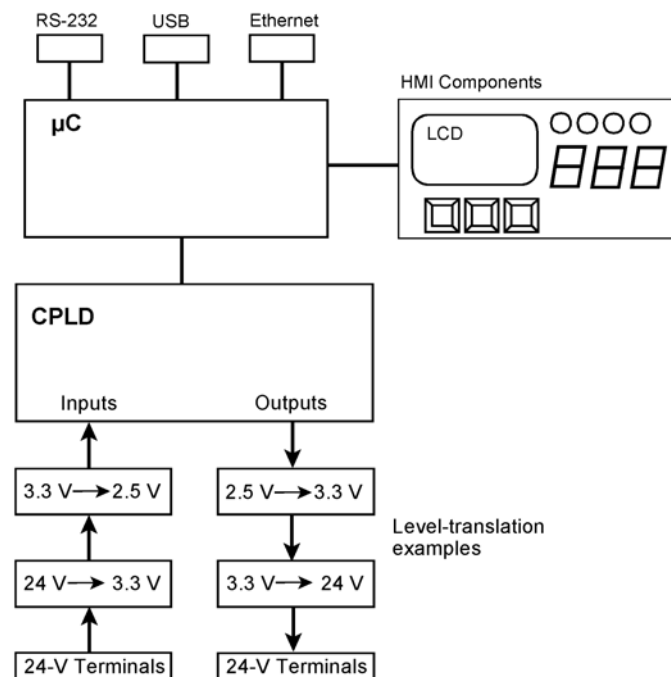
**Figure A7** IEC 61131-2 type 3 operating regions. Type 3 has been defined to support 2- and 3-wire sensors with reduced power consumption.

**The microcontroller-CPLD combo**



**Figure A8** Sometimes, it may be advantageous to employ a CPLD as the first stage of level conversion outside of the microcontroller. Refer, for example, to [32] to [34].

The IOs of some CPLDs are grouped in banks having their own VIO supply voltage. Thus, for example, the 1.8-V or 2.4-V signals of the microcontroller can be translated to 2.5-V LVCMOS levels, 3.3-V LVTTTL levels, and so on. Besides, the CPLD may swallow up most of the glue logic that otherwise would be spread over the PCB. Occasionally, the CPLD may accommodate even a coprocessor.



**Figure A9** Combining a microcontroller and a CPLD. Here, an evident, straightforward architecture is shown.

The principal question is which device is the master. In the first variant, it is the CPLD. The microcontroller is only used for initialization, diagnostics, communication, and the human-machine interface (for example, implemented by an LCD together with some keys and LEDs). In a second variant, the microcontroller is the master. It executes the application-specific software. The CPLD is merely an auxiliary device for level translation, marshalling, glue logic, and so on. Occasionally, it may accommodate even an accelerator or coprocessor.

The most straightforward approach is to connect all the microcontroller's signals that are to be translated to the CPLD, regardless of whether they belong to an industry-standard or peripheral interface (think of SPI, asynchronous interfaces, or the IOs of a counter-timer unit) or are to be used as programmable IOs. Thus the CPLD will be something like a patch or marshalling panel. It is, however, just as obvious to connect interface signals directly to the translation circuits.

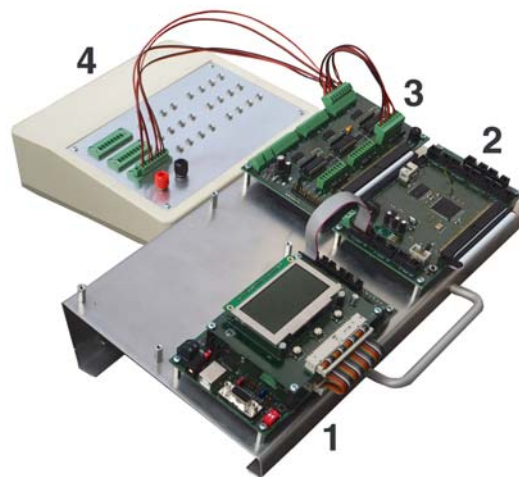
Concerning the programmable IOs connecting the microcontroller to the CPLD, I recommend contemplating some sort of architecture (in contrast to pure application-specific wiring, like between the components on a conventional PCB). Typical examples would be a data bus accompanied by some control and status signals or a simple shift register interface. The details may be application-specific; the basic ideas could be adopted from the typical bus systems of the

early microprocessors (think, for example, of Intel's 8051 or Motorola's 6800), from asynchronous SRAMs, and the like. For simple shift register interfaces, see also Figure 11 in the printed article.

The rationale behind this recommendation is that you will have to work with two different development environments, and you would certainly not want to be urged to modify the microcontroller software when changing something in the CPLD and vice versa. It goes without saying that true hardware-software co-design is state of the art. To be able to switch seamlessly between hardware and software requires, however, to move to FPGAs and their development environments, which are considerably more demanding (and expensive).

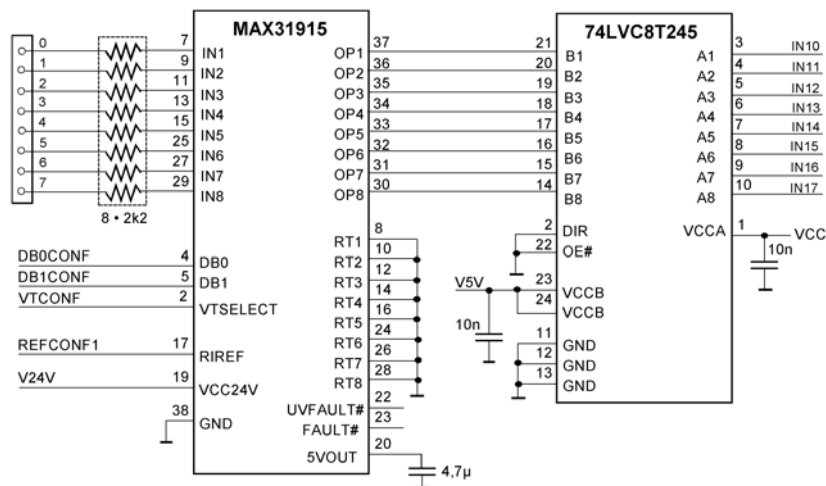
### The 24-V companion – an educational example

A 24-V microcontroller or CPLD would be a densely packed small PCB. When the basic architecture has been defined and the functional units developed, it is only a question of PCB design and manufacturing. Therefore, my own experiments had begun not with a tiny IOT module but with somewhat larger PCBs, one for each basic functional unit. The philosophy behind this approach and some of the modules I have described already in *Circuit Cellar* articles ([35], [36]).



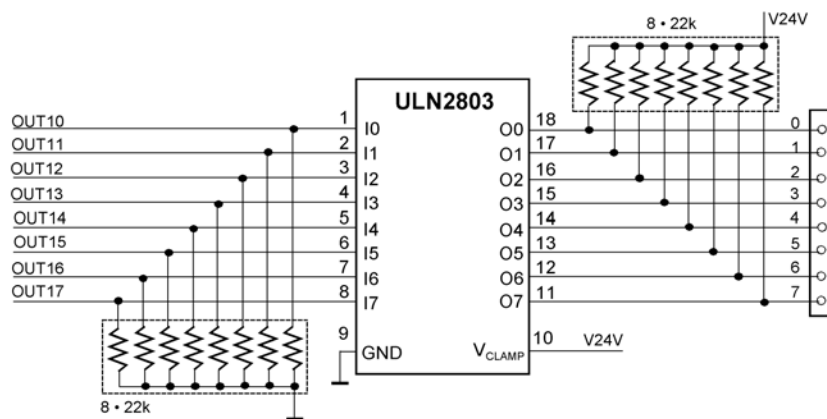
**Figure A10** An experimental IoT platform assembled from a microcontroller module (1), a CPLD module (2), and a voltage-translation module (3) dubbed the 24-V companion, connected to a 24-V indicator board (4). To run loopback tests, a cable connects an output port to the indicator board and an input port.

The microcontroller module carries an operating and display panel, thus constituting an HMI device. The CPLD module contains a Xilinx CoolRunner XC2C384 CPLD and an SRAM 256k • 16. The 24-V companion supports 24 inputs and 24 outputs, grouped in six 8-bit ports. The companion has a parallel logic interface, comprising 48 signals, that can be, via the so-called multi-purpose connector, attached to the CPLD module or appropriate microcontroller modules. The multi-purpose connector has been mentioned in my article [35]. The interface between the microcontroller and the CPLD comprises 16 signals that may be used for application-specific wiring. I prefer, however, a somewhat architected solution with an 8-bit data bus and up to 8 control and status signals. The 24-V indicator board is a purpose-built auxiliary device displaying the status of 24 output signals, grouped in three ports of eight. It consists essentially of 24-V LED signal lamps wired to headers. All components are mounted in the front panel of a sloped enclosure.



**Figure A11** One of the companion's three input ports. The RT outputs may be connected to LEDs. Without LEDs, they must be connected to ground to close the current return paths. The translator's configuration is to be set via jumpers on the PCB. DB0CONF, DB1CONF select the time constant of the glitch filter. VTCONF selects the input trip point (CMOS or IEC61131-2). REFCONF1 to 3 are connected to reference resistors for current limiting. The current limit may be set between 0.5 and 6 mA.

Input translation is done in two stages, from 24 V to 5 V by a MAX31915 ([D6]) and from 5 V to 3.3 V by a 74LV8T245 ([D19]). Translation ICs with parallel interfaces have been chosen because the companion should preferably be attached to a CPLD.



**Figure A12** One of the three output ports.

The output stages are straightforward ULN2803 Darlington drivers. To ensure definite signal levels even when no module or load is attached, the logic and 24-V signals are connected to pull-down and pull-up resistors, respectively.

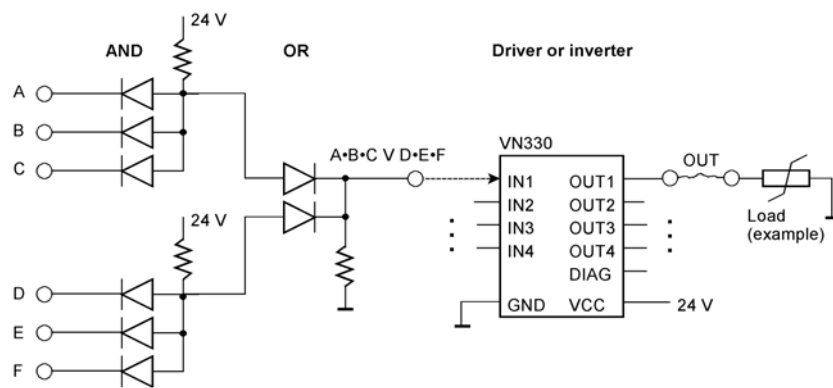
### Integrated level translators

Our block diagrams – in the printed article and here – are based on actual data sheets. They have been, however, considerably simplified and redrawn to illustrate the essential principles of operation. Who wants to know more, we refer to the data sheets, whitepapers, and application

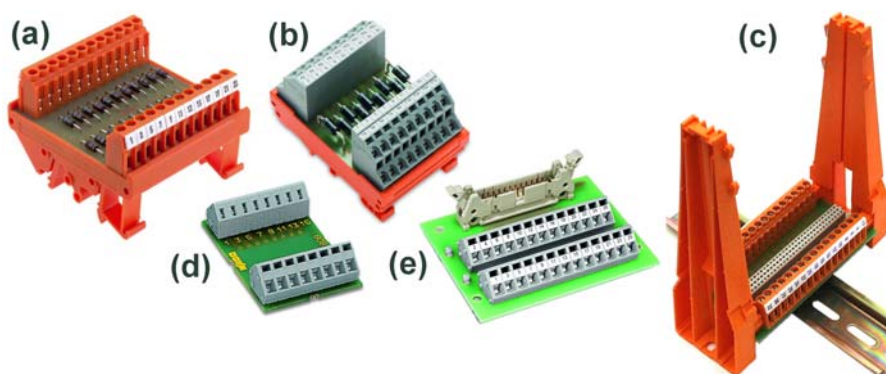
notes of the semiconductor manufacturers. The references [24] to [31] and [D1] to [D19] are thought of as introductory examples.

### Simple 24-V logic

Some decades ago (we speak of the Fifties and Sixties), control equipment manufacturers offered transistorized pluggable modules performing logic functions, like gates, flip-flops, counters, and so on. The modern equivalents are essentially very small PLCs, down to programmable relays. Occasionally, however, the need arises to implement hard-wired logic functions at the 24-V level without resorting to PLC programming. The problem can be solved by developing application-specific modules or by tinkering with diodes, transistors, driver modules, and so on. Manufacturers know this need and offer appropriate building blocks. As an alternative solution, we propose the 24-V CPLD.

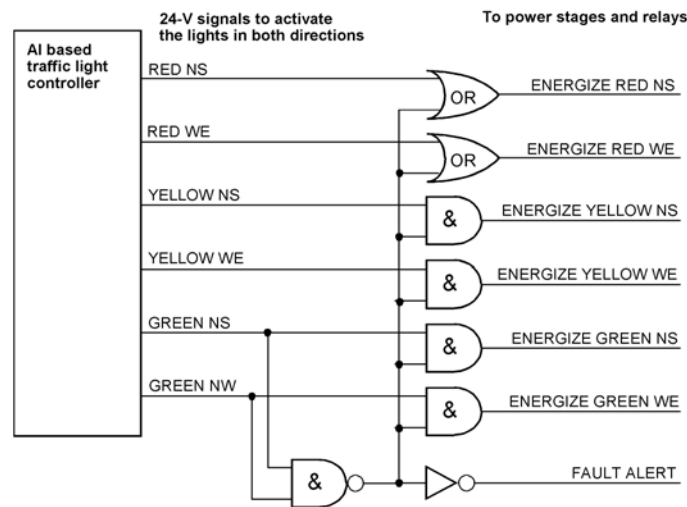


**Figure A13** Diode logic to implement AND and OR functions. The V330 is a quad high-side driver IC (smart power solid state relay), driving resistive or inductive loads connected to ground ([D20]). To invert signals, we can make use of transistor stages, low-side driver ICs or solid-state relay modules.



**Figure A14** Only a few examples of appropriate modules (from Weidmueller, Wago, and Appoldt). Above all, they are mechanical building blocks to clip onto DIN rails. More or less craftwork is required to implement the desired functions. (a) and (b) show modules with diodes. (c) connects a pluggable PCB to the field wiring. (d) is an uncommitted module to accommodate application-specific components. The rear connector of (e) allows to insert an application-specific PCB or to attach external circuitry via a ribbon cable. A 24-V CPLD may have, for example, a form factor similar to (a) or (c).



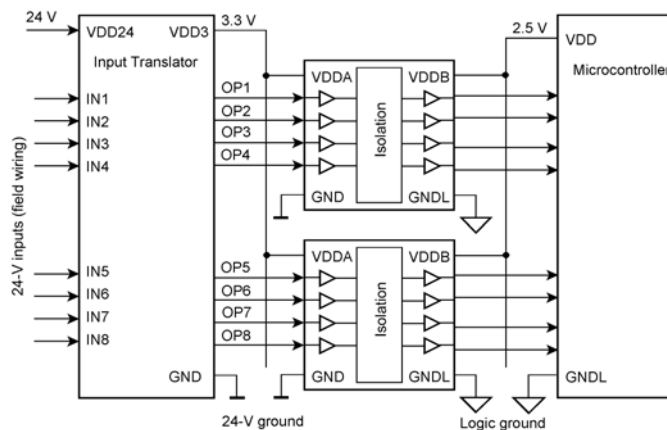


**Figure A15** Supervising traffic light control – a considerably simplified but plausible example of 24-V logic. NS = North/South, WE = West/East.

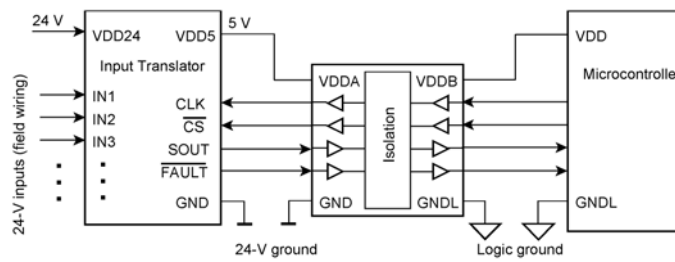
A sophisticated AI-based system controls the traffic lights on an intersection. What must never occur is that all the green lights on the intersection lanes switch on simultaneously. Here, all red lights will switch on if this fault occurs. Improvements are obvious. For example, a timing relay could, after an appropriate time period, disable all the lights. Thus the traffic may resume whereby the drivers have to heed the right of way as stipulated in the traffic regulations. A microcontroller-CPLD combo could do much more than a few logic gates. For example, it could take over the traffic light control and keep the traffic going by an unsophisticated and stupid but guaranteed error-free algorithm.

**Isolation**

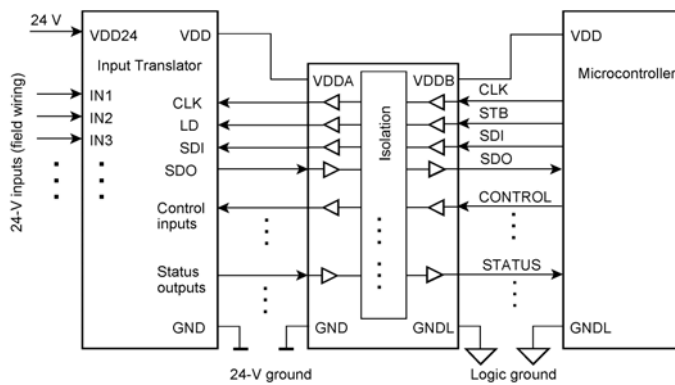
IC manufacturers recommend inserting the isolation between the translator circuits and the processing platform (which is typically a microcontroller or an FPGA).



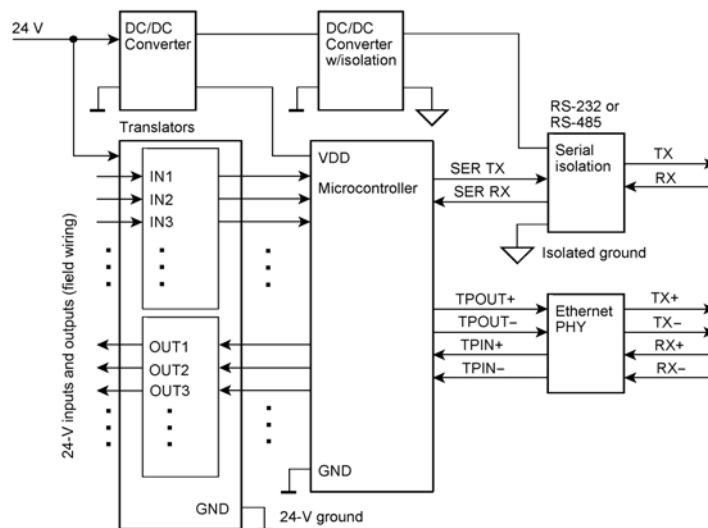
**Figure A16** A parallel interface with isolation devices inserted. For an example refer to [D10].



**Figure A17** This input translator has an SPI interface confined to read the input states (input serializer). Isolation is done by one IC supporting both SPI signal directions. For an example refer to [D1].



**Figure A18** This is an example of a shift register interface, supplemented by further inputs and outputs. Here, the isolation circuitry is shown as one building block. In practice, it must be implemented by two or more appropriate ICs. For examples of shift register interfaces refer to [D14] to [D16].

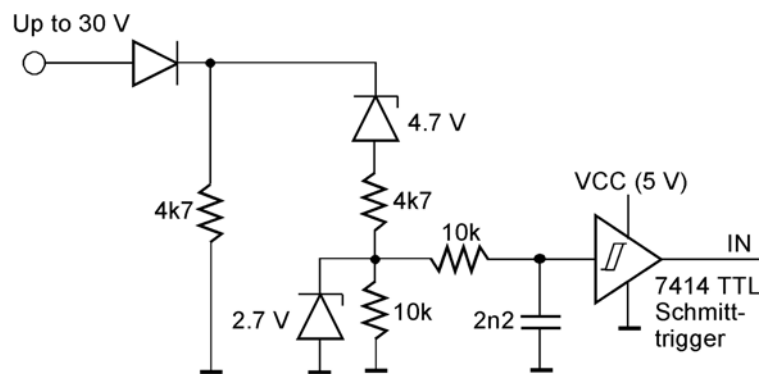


**Figure A19** When designing tiny modules, like our 24-V microcontrollers and CPLDs, the number of components is to be minimized to keep the PCB small and to ensure high reliability. Therefore, it may be advantageous to connect the whole module to the field wiring ground and isolate only the power supply and the external interfaces. In some cases, the transformers of the DC/DC converters and the Ethernet PHY could provide sufficient isolation.

### Translation with discrete components

Level translation problems can be solved with discrete or SSI components, such as Zener diodes, bipolar junction transistors (BJTs), field-effect transistors (FETs), and comparators. Zener diodes and MOSFETs are well-suited to translate 24-V to logic signals (down to 3.3 V or below). BJTs and comparators may be employed in both directions.

Designing with discrete components is an art in itself. Regrettably, today it is only seldom taught. Even textbooks which are otherwise excellent, deal with those topics quite sketchily. Here, we can only touch a few of the most basic circuits. For more, we refer to appropriate sources provided by the semiconductor manufacturers and the vintage literature.



**Figure A20** An IEC 61131-2 compliant input translated using Zener diodes ([37]).

The 4.7-V Zener begins to conduct if the input voltage exceeds approx. 5 V, thus guaranteeing a LOW level as long as the input voltage is less than 5 V. The 2.7-V Zener limits the input voltage of the 7414 Schmitt trigger. The 10k/2n2 combo acts as a low-pass or de-glitching filter.

### Watch out for anomalous conditions at the inputs

More intricate problems like ESD, power line interference, crosstalk, and so on we cannot discuss here. They are typical of true factory floor environments. When pursuing humble hobbyist or educational projects, the environment will not be that harsh. There are, however, two conditions you should consider even under those benign circumstances: The first is no signal at all, that is, an open input. The second is a high-impedance (tri-stated) signal. This condition may occur during initialization or as a consequence of faults. A microcontroller running self-tests, communicating via the network, and the like before initializing its output ports may cause such signals to float for a prolonged time. Under both conditions, you should guarantee your translation circuit sees a definite LOW or HIGH input level. Which of both levels to choose as the default depends on the particular application.

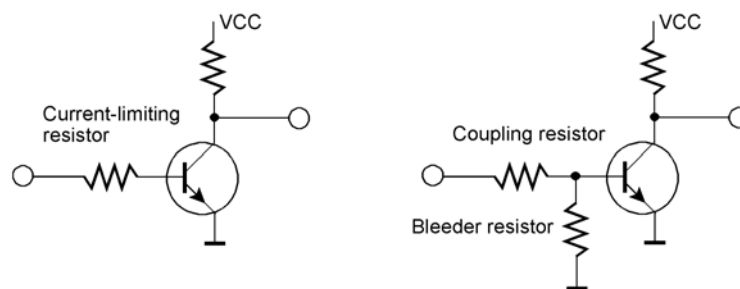
### How to drive a BJT

The decisive data sheet value is the Base-Emitter Saturation Voltage  $V_{BE(sat)}$ . Small-signal BJTs are rated typically between 0.7 V and somewhat above 1 V. To keep the transistor safely in the OFF state, the base-to-emitter-voltage should be kept well beyond  $V_{BE(sat)}$ , say, for example, at approx. 0.3 V. To switch it on, the signal source should deliver a voltage well above 1 V. Then

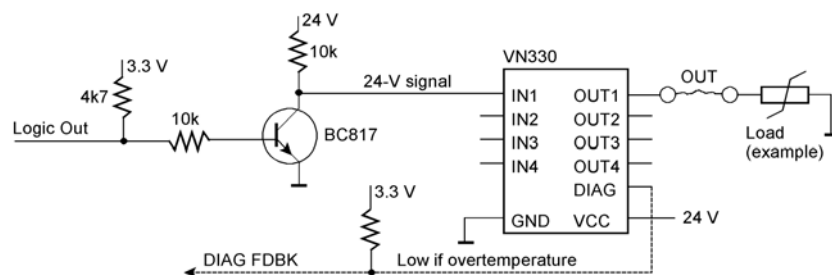
the current path from the base to the emitter will behave like a diode operated in forward direction. Therefore, it is necessary to limit the base current. When no anomalous conditions will occur, especially when the signal source is a CMOS logic output, then the current-limiting resistor alone may suffice. Its value according to a proven rule of thumb:

(Signal voltage –  $V_{BE(sat)}$ ) divided by a tenth of the output current.

For 24-V inputs, however, you would be better off with the voltage divider, eventually combined with a Zener-based voltage limiter.



**Figure A21** Employing a BJT. The two most basic circuits. Some manufacturers offer transistors with a built-in current-limiting resistor or coupling/bleeder resistor combo ([38]).



**Figure A22** An application circuit translating 3.3-V signals to 24 V ([37]). The pull-up resistor keeps the transistor switched ON when the input is floating. Consequently, the VN330 will not energize the attached load.

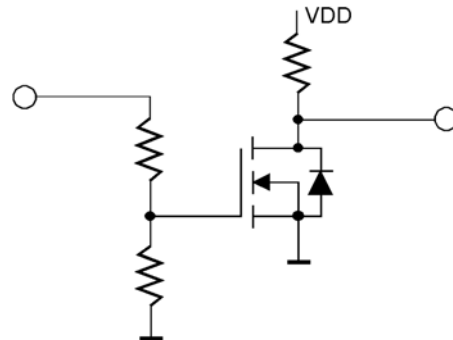
### The BJT switched ON

The most important parameter is the Collector-Emitter Saturation Voltage  $V_{CE(sat)}$ . Small-signal BJTs have typical data sheet values around 0.2 V. However, to keep the voltage this low, the transistor must be operated in saturation, that is, overdriven by a base current sufficiently high. (Hence we divide the output current by 10 and not by the current-gain parameter  $h_{21E}$  or Beta in the data sheet.)

### How to drive a MOSFET

In contrast to the BJT, which is controlled by the base current, the MOSFET is controlled by the gate voltage. To keep the transistor safely in the OFF state, the gate-to-source voltage should be kept well below the Gate-Source Threshold Voltage  $V_{GS(th)}$ . Typical values are between somewhat under 1 V up to somewhat around 5 V. To switch the transistor on, you have to consider the minimum gate voltage that guarantees the data sheet value of the Drain-Source Resistance  $R_{DS(on)}$ .

10 V is a common value. Observe that the  $V_{GS(th)}$  data sheet value relates not to a transistor completely switched ON but to the transitional range between OFF and ON.  $V_{GS(th)}$  is often specified as a gate voltage permitting a mere weak drain current to flow (for example, as low as 250  $\mu\text{A}$ ).



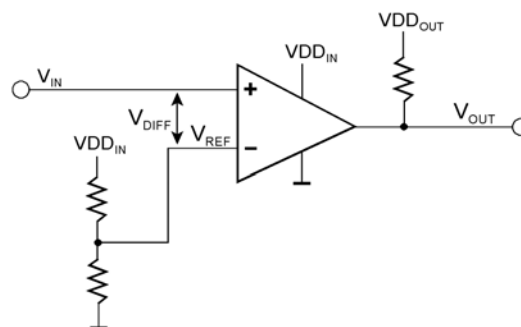
**Figure A23** Employing a MOSFET. The most basic circuit.

### The MOSFET switched ON

FETs are voltage-controlled variable resistors. The voltage drop  $V_{DS}$  between drain and source results from the drain current flowing through the drain-to-source resistance ( $V_{DS} = I_D \cdot R_{DS(on)}$ ). So keep the gate voltage high enough and the drain current only as high as necessary.

### Level translation with comparators

The comparator is a high-gain, non-feedback differential amplifier. The output should assume only one of two levels (Low or High), depending on the voltage difference  $V_{DIFF}$  between the inputs. Many comparator ICs have open-collector or open-drain outputs. The output voltage swing may be as large as the appropriate data sheet parameter permits; it does not depend on the comparator's supply voltage. Thus, for example, a comparator supplied with 24 V may output 3.3-V signals.



**Figure A24** Employing a comparator with an open-drain or open-collector output. The most basic circuit. The comparator's supply voltage  $V_{DDin}$  corresponds to the input signal level.

It seems straightforward to employ a comparator. Connect one input to the signal to be translated and the other input to an appropriate reference voltage, which may be provided by a simple voltage divider. There are, however, a few caveats. Here, we will only mention the two most important: the slew rate of the input signal and the input common-mode range.

A comparator has no built-in snap-action mechanism. The threshold effect results solely from the high voltage gain, causing even a small difference in input voltages to overdrive the amplifier. If this difference is very small, however, there will be no overdriving. Parasitic feedback effects could cause the output even to oscillate. On the other hand, if this so-called linear region is traversed fast enough, the comparator will find no opportunity to switch back and forth. Hence only a single signal edge will occur. Thus you have to consider the rise and fall times of the input signal. If they may be too slow, the simple circuit will not work properly. Well-proven remedies you will find in the literature, for example, the Schmitt-trigger circuit or to introduce a particular input behavior, called hysteresis ([39], [40]).

The input common-mode range is typically somewhat smaller (at least some hundreds of millivolts) than the voltage difference between both power supply terminals. This may be a problem if the negative power terminal is connected to the ground (single-ended operation). If the LOW level of your input signal is nearly equal to 0 V (for example, if it is driven by a CMOS logic output switching rail-to-rail), you should prefer a comparator that will function properly in such a case. This property is termed ground sensing in single-ended applications (or something like that).

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*Some manufacturers of I/O modules and industrial PCs:*

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Dataforth Corporation: <https://www.dataforth.com/default.aspx>

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