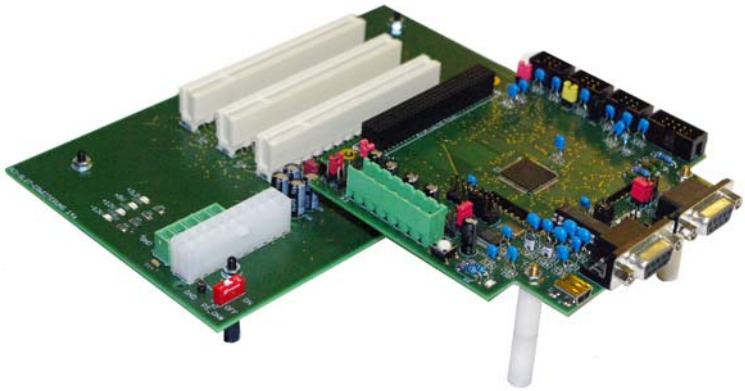
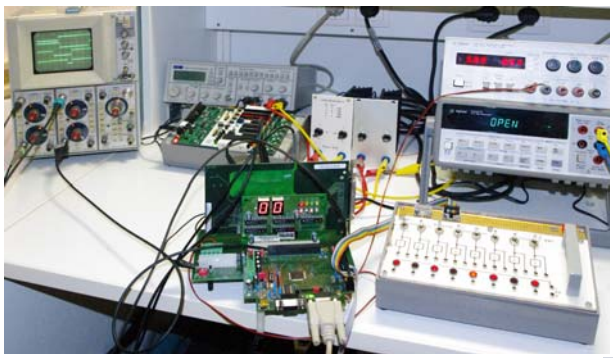
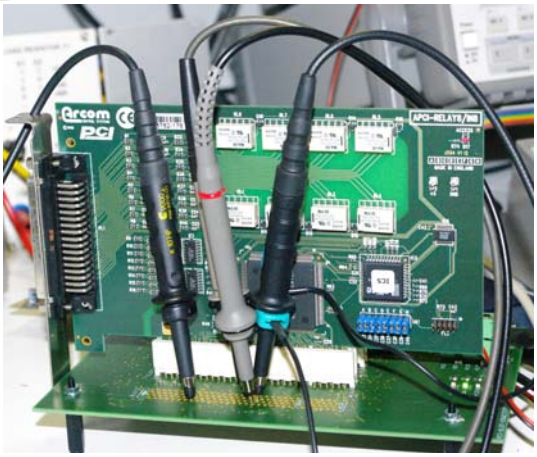
PCI Host Controller 14a
Hardware Reference

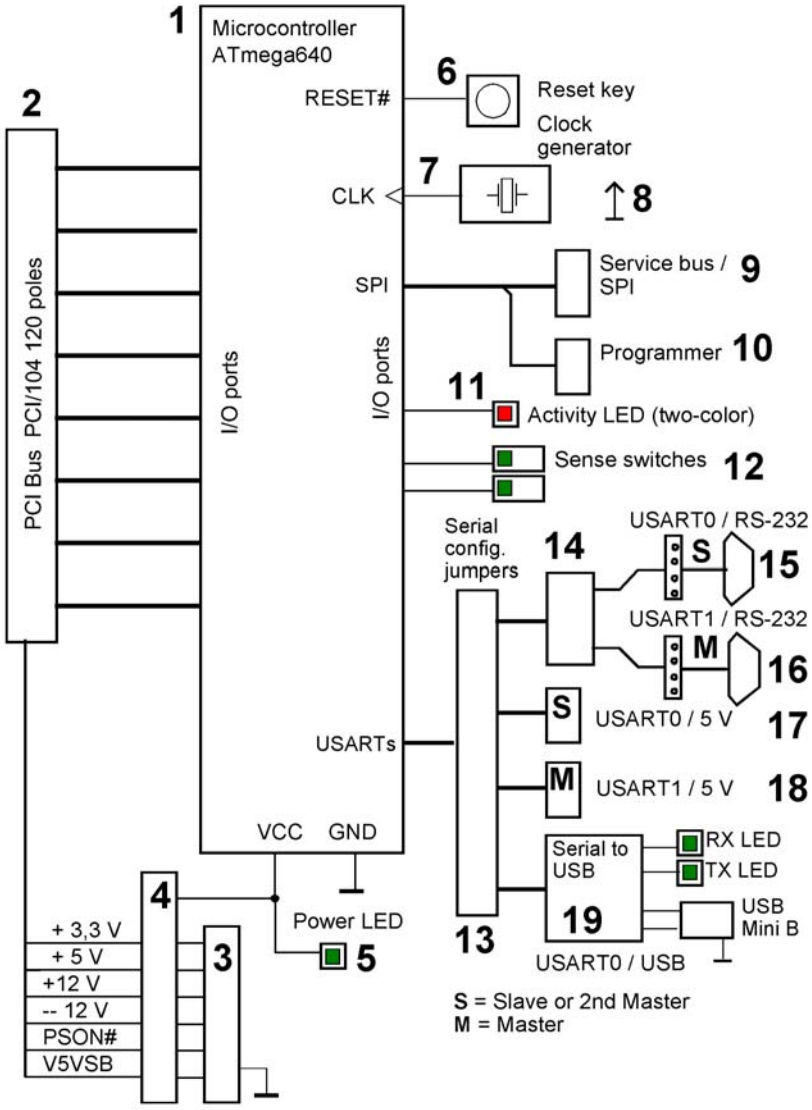
Release 1.2 (October 16, 2017)

Purpose:
Host Controller to support the PCI bus according to the PCI/104 specification. Alternatively, a general-purpose microcontroller module in the PCI/104 form factor, providing 62 freely programmable I/O signals on a 120-pole stackable connector. The module supports two serial interfaces and 8 freely programmable I/O signals, organized as the so-called service bus. Both serial interfaces provide for 5-V and RS-232 signalization. One of the serial interfaces can be accessed via a USB-to-serial converter. The service bus can be programmed to support the SPI interface, allowing the module to operate as master or slave device.









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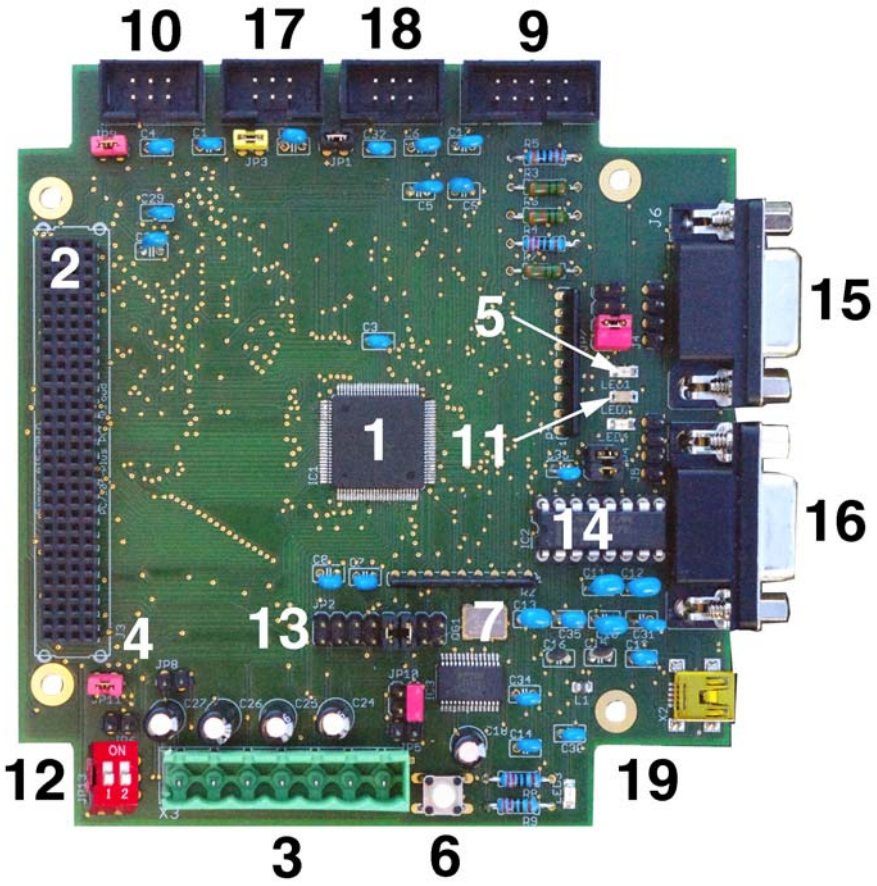

Note:
The block diagram corresponds to release 1.2, the photo depicts the first protoptye (V1), release 1.1.

Microcontroller (1)
The board can be populated with an microcontroller Atmel ATmega 620, 1280 or 2560 in a TQFP100 package. 64, 128 or 256 kBytes Flash, 8 kBytes RAM, 4 kBytes EEPROM, maximum clock frequency 16 MHz.

PCI/104 connector (2)
All PCI signals supported by the module are attached to this connector. The pin assignment corresponds to the PCI/104 specification.

Note :
Details see below under "The PCI Bus" (page 7).

Power supply connector (3)
This terminal block has a pin pitch of 150 mils = 3.81 mm. Any connector type with appropriate footprint may be inserted. It allows connecting all the supply voltages required according to the PCI specifications (+ 3,3 V; + 5 V, + 12 V – 12 V) as well as a standby voltage V5VSB and the power-on signal PSON#, which are typical of ATX power supplies. The connector may be omitted, when power can be supplied via other connectors.

Power supply configuration (4)
Power must be supplied from outside. There is no voltage regulator and no anti-reversal protection. The board has only one operating voltage, which must be equal to the PCI signaling voltage to be supported (5 V or 3,3 V). The power supply configuration must be set by various jumpers. Details see below under "Power Supply Configuration" (page 12).

Power LED (5)
One of the most basic troubleshooting aids is an indication, whether a device is powered or not.

Reset key (6)
The reset key is an inexpensive, but convenient means to facilitate debugging and troubleshooting.

Note:
Key actuation will reset only the microcontroller. To reset the bus devices, an PCI RST# pulse must be generated by software.

Clock generator (7)
A crystal clock generator allows to operate the microcontroller up to its maximum clock frequency. The nominal clock frequency is 16 MHz.

Ground test point (8)
A ground test point can be inserted to support oscilloscope attachment and the like.

Service bus header (9)
The service bus comprises 8 signals. The service bus is composed of 4 bit-positions from port B and 4 bit-positions from port D. All bits are freely programmable. It can be employed to implement an SPI interface (master or slave), accompanied by 4 additional signals (which can be used to select SPI peripherals or to trigger interrupts). The header comprises VCC and GND pins. They can be used to power external circuitry or to feed the module.

The service bus:

7	6	5	4	3	2	1	0
SRVBUS7	SRVBUS6	SRVBUS5	SRVBUS4	SRVBUS3	SRVBUS2	SRVBUS1	SRVBUS0
Port B3	Port B2	Port B1	Port B0	Port A7	Port A6	Port A5	Port A4
MISO	MOSI	SCK	SS#				

Programming header (10)
The pin assignment corresponds to that of the industry-standard Atmel programmers. The header comprises VCC and GND pins. They can be used to power external circuitry or to feed the module. The VCC rail connection is controlled via pin header JP1.

Activity LED (two-color) (11)
The activity LED can be controlled by two microcontroller signals, LED_A and LED_B. These signals are used to enable the Device Detection feature, too.

LED_A	LED_B	Effect
Low	Low	LED off
Low	High	LED lights green
High	Low	LED lights red
High	High	LED off

Sense switches (12)
The on-off position of two switches can be sensed by two microcontroller signals, SENSE_SW1 and SENSE_SW2. These signals are low-active.

Note:
Instead of dual-in-line (DIL) switches, pin headers (JP12, JP13) may be inserted, allowing to attach external switches in a more convenient location (e.g., on a front panel).

Serial interfaces configuration (13)
The serial interfaces are configured by jumpers via the pin headers JP5 to JP8.

Note :
Details of the serial interfaces configuration see below under "Serial Interfaces" (page 9) and "Configuring the PCI Host Adapter" (page 10).
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RS-232 level converter (14)
Level conversion is done by a MAX232 level converter IC.

USART0 RS-232 slave connectors (15)
The RS-232 signals belonging to USART0 are to be attached via pin headers o a 9-pole D-sub connector. The VCC and GND pins can be used to power external circuitry or to feed the module.

USART1 RS-232 connectors (16)
The RS-232 signals belonging to USART1 are to be attached via pin headers o a 9-pole D-sub connector. The VCC and GND pins can be used to power external circuitry or to feed the module.

USART0 5-V signalization header (17)
This header is connected to USART0. The header comprises VCC and GND pins. They can be used to power external circuitry or to feed the module. The serial signals are directly connected to the microcontroller.

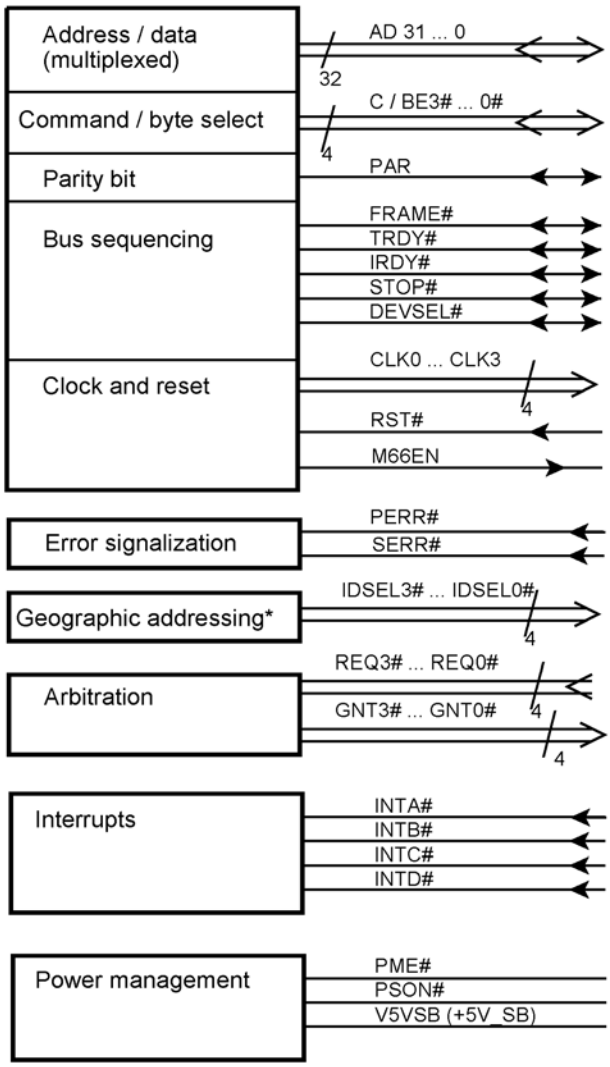
USART1 5-V signalization header (18)
This header is connected to USART1. The header comprises VCC and GND pins. They can be used to power external circuitry or to feed the module. The serial signals are directly connected to the microcontroller.

Note:
The VCC rail connection in both headers (17), (18) is controlled via pin header JP3.

USB-to-serial converter (19)
USB-to-serial conversion is done by a FT232RL IC. The USB connector is of the Mini-B type. To facilitate troubleshooting, two LEDs are provided, indicating transmit and receive activities (TX LED, RX LED).

The PCI Bus

The legacy PCI bus is a general-purpose 32-bit bus system characterized by combined address and data signals (address / data multiplexing), multi-master capability, program-controlled address assignment ("plug-and-play"), and synchronous operation. In the bus cycles, the signals are valid only with regard to the Low-to-High edges of a common bus clock. The nominal clock frequency is 33 MHz. However, the PCI specification stipulates devices to be operational even with a bus clock of zero Hz. In other words, all PCI cards and modules must be able to be operated statically. PCI has been designed as a motherboard bus. A motherboard allows to route point-to-point connections to each device. In this way, geographic addressing, interrupt signalization, and bus arbitration was implemented. However, a PC/104 system is a stack of modules, where there is no simple way to make point-to-point connections. To solve this problem, the stackable connectors provide contacts for four instances of each point-to-point signal.



*: Used only for device identification and address assignment (plug-and-play configuration).

PCI bus signals	Function	Notes
AD31...0	Address and data bus (multipexed)	A bus transaction begins with address phase. One or more data phases follow
C/BE#3...0	Command / Byte enable	Signalizes the command during address phase, enables data bytes during data phase
PAR	Parity	Even parity across AD31...0 and C/BE3...0
FRAME#	Bus cycle frame	Indicates the begin of a bus transaction. Remains active until the final data cycle. Driven by the initiator (master)
TRDY#	Target ready	Indicates that the target (slave) is ready to complete the current data phase
IRDY#	Initiator Ready	Indicates that the initiator (master) is ready to complete the current data phase
STOP#	Stop transaction	The target (slave) signals the transaction to terminate
DEVSEL#	Device select	Signalized by the device which has recognized the current address
CLK3...0	Bus clock	
RST#	Bus reset	
M66EN	Enable 66 MHz operation	On this board, the signal is always inactive (Low)
PERR#	Data parity error	
SERR#	Address parity error	
IDSEL3#...0#	Initialization device select	To select a device during configuration transactions (geographic addressing)
REQ3#...0#	Bus master request	Signalized by a device which will become a bus master (initiator)
GNT3#...0#	Bus cycle has been granted	Reply to a bus request. Allows the requesting device to claim the bus and act as a bus master (initiator). Signalized by the arbitration circuitry
INTA#...INTD#	Interrupt request	Four interrupt request signals
PME#	Power management event	A request signal driven asynchronously by the devices to trigger power management event
PSON#	Power supply on	Signal to switch an ATX-type power supply unit on or off
+5V_SB (V5VSB)	+ 5 V standby voltage	The standby voltage of an ATX-type power supply unit

Serial Interfaces

Two USARTs
The microcontroller provides two serial interface controllers, called Universal Synchronous and Asynchronous Receivers and Transmitters (USARTs).

Two modes – slave and master
Th serial interfaces can be employed to connect the module upstream to a host machine or downstream to attached devices. In upstream connection, the module is seen as Data Communications Equipment (DCE) and operated upon as a slave device. In downstream connection, the module acts as Data Terminal Equipment (DTE) and behaves as the master device.

Serial signalization
There are three flavors of serial signalization: the 5-V signalization, the RS-232 signalization and the USB signalization. At the USB, the module can act only as a device. Hence, the USB attachment is available only for slave operation at USART0.

USART 0	USART 1
Slave 5 V	Master 5 V
Slave RS-232	Master RS-232
Slave USB	
2nd Master 5 V	
2nd Master RS-232	

Interface	5-V connector		RS-232 pin header		RS-232 D-sub 9 connector		
	TX	RX	TX	RX	TX	RX	Gender
Slave	Pin 1	Pin 3	Pin 3	Pin 2	Pin 2	Pin 3	Female
Master	Pin 3	Pin 1	Pin 2	Pin 3	Pin 3	Pin 2	Male

Slave and master with regard to RS-232 signalization

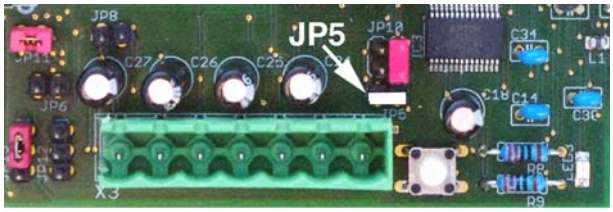
- A Slave is a DCE device, like every RS-232 device downstream of a personal computer. The RS232-connector is a female DSub9 connector with TX on pin 2, RX on pin 3.
- A Master is a DTE device. The RS232-connector is a male DSub9 connector with TX on pin 3, RX on pin 2. If J8 is a female DSub9, an appropriate gender changer may be required.

Configuring the PCI Host Adapter

JP1 – VCC to programming header J1 (10)
Insert jumper JP1 to connect the programming header J1 (10) to VCC.

JP3 – VCC to 5-V serial headers J4 (17) and J5 (18)
Insert jumper JP3 to connect the 5-V serial headers to VCC.

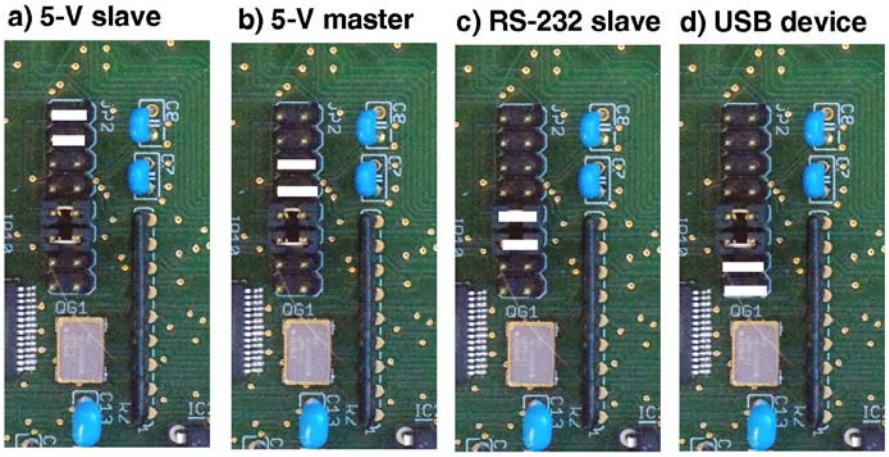
JP5 – Power the module from the USB connector
Insert jumper on pin header JP5 if the module is to be powered by the USB.



Note:
If the module is operated as a USB device (in contrast to attaching to a USB charger or power bank), this method of drawing power is not compliant with the USB standards. Use it only for bring-up and experimental purposes. In all cases, USB current should not exceed approx. 800 mA.

JP2 – USART0 configuration
Insert two jumpers to connect the desired serial signals to USART0. One of the following configurations can be selected:

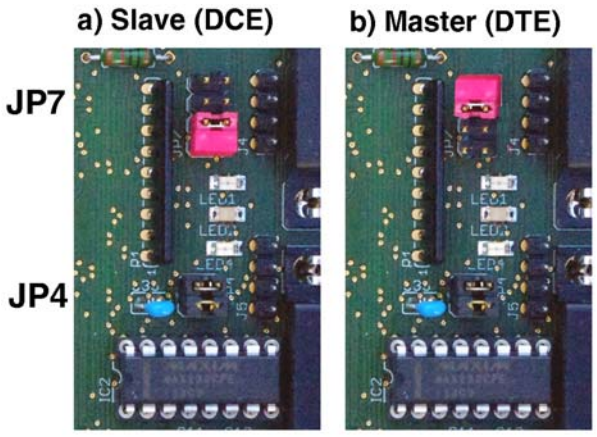
a) 5-V slave,
b) 5-V master (2nd master),
c) RS-232 slave,
d) USB device (slave).



JP4 – using USART1 with R2-232 signalization
If USART1 is to be configured for RS-232 signalization, insert two jumpers to connect the USART signals to the MAX232 level converter.

JP7 – configuring the RS-232 attachment of USART0
This interface can be operated in one of two modes. Insert two jumpers accordingly:

a) Slave or DCE. TX on pin 3, J4 and pin 2, J6. RX on pin 2, J4 and pin 3, J6.
b) Master or DTE. TX on pin 2, J4 and pin 3, J6. RX on pin 3, J4 and pin 2, J6.



Power Supply Configuration

Which supply voltages are required?
The module alone needs only VCC = 5 V or 3,3 V. In a PCI configuration, the system components determine over the other supply voltages. Specification-compliant PCI supply voltages may be applied via the power supply connector J11 or the PCI/104 connector J10.

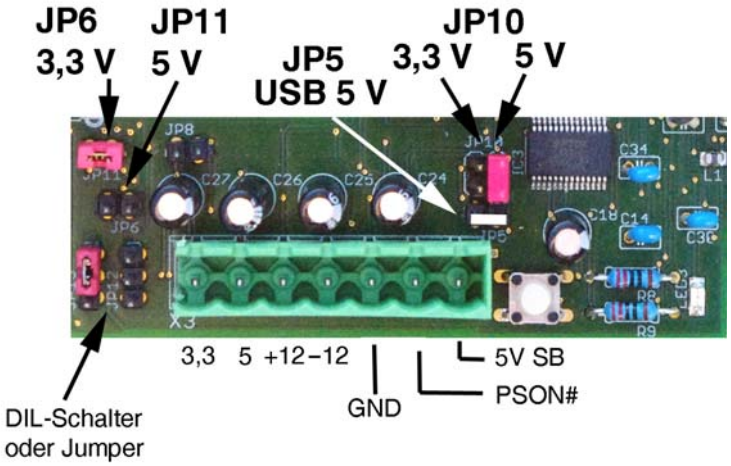
Power sources for 5-V operation:

a) the power supply connector J11,
b) the PCI/104 connector J10,
c) external power fed via the service bus, serial or programming connectors,
d) the USB.

Power sources for 3,3-V operation:

a) the power supply connector J11,
b) the PCI/104 connector J10.

Select the I/O and operating voltage by appropriately inserting a jumper on JP10 (5 V or 3,3 V). If power is supplied via the power supply connector J11, or the PCI/104 connector J10, then disconnect USB power (JP5). Check the power supply jumpers JP1, JP3 of the other peripheral connectors.



Notes:

1. The preferred operating and I/O voltage is 5 V. 3,3-V operation requires populating the board with appropriate components, above all a 3,3-V clock generator and a MAX3232 level converter. Devices attached to the service bus, the programming connector, or the serial headers must support 3,3-V signaling.
2. JP6, JP8, JP9, and JP11 have been provided for bring-up and experimenting. Make connections by inserting jumpers on JP6 and JP11. JP8 and JP9 are not used. All those headers will be omitted in future releases.

3. The power supply via the USB connector does not comply with the USB standard. If attached to a USB host, this provision should be used only for testing, experimenting and the like.
4. Power supply devices with USB connectors can be used (e.g., chargers or so-called power banks). However, do not feed a larger PCI system via this connection, because PCB traces of the USB attachment cannot carry large currents. Current should not exceed approx. 800 mA.

The Programming Interface

Port A

7	6	5	4	3	2	1	0
SRVBUS 3	SRVBUS 2	SRVBUS 1	SRVBUS 0	LED_B	LED_A	res.	res.
Initialize service bus according to intended use				Output	Output	Input	Input

Port B = Connectors J2 und J6:

7	6	5	4	3	2	1	0
CLK3	CLK2	CLK1	CLK0	SRVBUS 7	SRVBUS 6	SRVBUS 5	SRVBUS 4
OC0A/1C	OC1B	OC1A	OC2A	MISO	MOSI	SCK	SS#
Output	Output	Output	Output	Initialize service bus according to intended use			

Port C

7	6	5	4	3	2	1	0
SSW1#	SSW0#	PAR	DEVSEL#	STOP#	IRDY#	TRDY#	FRAME#
Input	Input	TS	STS	STS	STS	STS	STS

Port D

7	6	5	4	3	2	1	0
INTD#	INTC#	INTB#	INTA#	TX1	RX1	SERR#	PERR#
Initialize service bus according to intended use				Output	Input	Input	STS

Initialize unused service bus signals as inputs with internal pull-up's activated.

Port E

7	6	5	4	3	2	1	0
REQ3#	REQ2#	REQ1#	REQ0#	res.*	res.*	TX0	RX0
Input	Input	Input	Input	Input	Input	Output	Input

Up to release 1.2: bit 2 = XPRSNT1#, bit 3 = XPRSNT2#

Port F

7	6	5	4	3	2	1	0
IDSEL3	IDSEL2	IDSEL1	IDSEL0	GNT3#	GNT2#	GNT1#	GNT0#
Outputs							

Port G

5	4	3	2	1	0
PME#	RST#	C/BE3#	C/BE2#	C/BE1#	C/BE0#
Input	Output	TS	TS	TS	TS

Port H

7	6	5	4	3	2	1	0
AD07	AD06	AD05	AD04	AD03	AD02	AD01	AD00
Bidirectional address/data bus (TS)							

Port J

7	6	5	4	3	2	1	0
AD15	AD14	AD13	AD12	AD11	AD10	AD09	AD08
Bidirectional address/data bus (TS)							

Port K

7	6	5	4	3	2	1	0
AD23	AD22	AD21	AD20	AD19	AD18	AD17	AD16
Bidirectional address/data bus (TS)							

Port L

7	6	5	4	3	2	1	0
AD31	AD30	AD29	AD28	AD27	AD26	AD25	AD24
Bidirectional address/data bus (TS)							

Notes:

1. Initialize reserved signals and unused service bus signals as inputs with internal pull-up resistors activated.
2. The module acts as the central resource, park master, and initiator (bus master). Bus signals will be driven or received according to PCI specification 2.2 / 2.3.
3. STS = Sustained Tri-State. In the idle state, the module will not drive these signals. They will be held on a High level by pull-up resistors (sustained tri-state).
4. TS = Tri-State. These signals have no pull-up resistors. In the idle state, they will be driven (parked) on stable levels (Low or High).