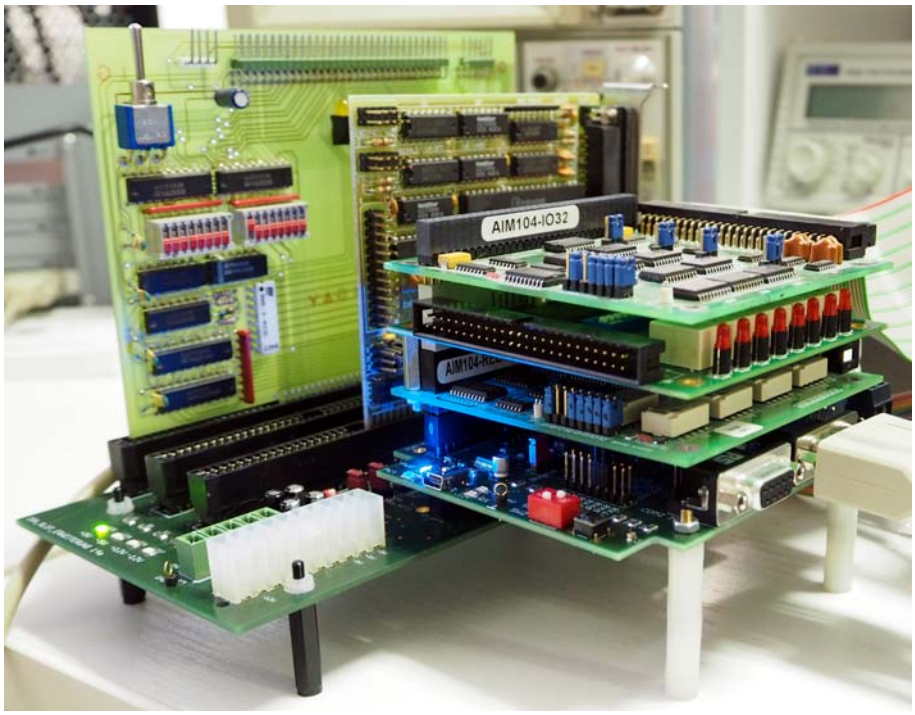
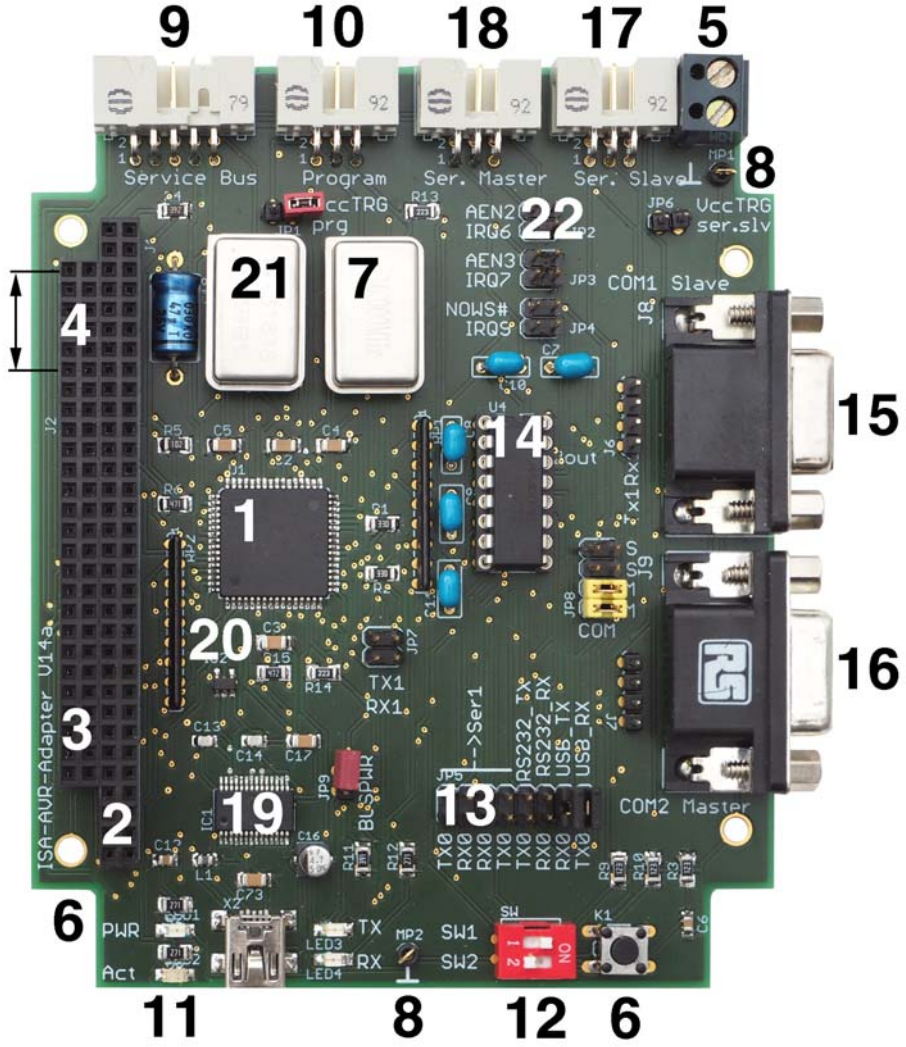
ISA Host Controller 15a
Hardware Reference

Release 1.2 (October 16, 2017)

Purpose:
Host Controller to support the ISA bus according to the PC/104 specification. Alternatively, a general-purpose microcontroller module in the PC/104 form factor, providing 38 freely programmable I/O signals on a 64-pole stackable connector. ISA bus operation is confined to 8-bit I/O cycles and 16-bit I/O addressing. The module supports two serial interfaces and 8 freely programmable I/O signals, organized as the so-called service bus. Both serial interfaces provide for 5-V and RS-232 signalization. One of the serial interfaces can be accessed via a USB-to-serial converter. The service bus can be programmed to support the SPI interface, allowing the module to operate as master or slave device. The PCB can accommodate both PC/104 connectors (64 and 40 poles). It can be stacked onto PC/104-compliant base boards. When the ISA base board 14a is employed, a supplementary connector can be inserted, providing for power supply connections and geographic addressing of the ISA slots.





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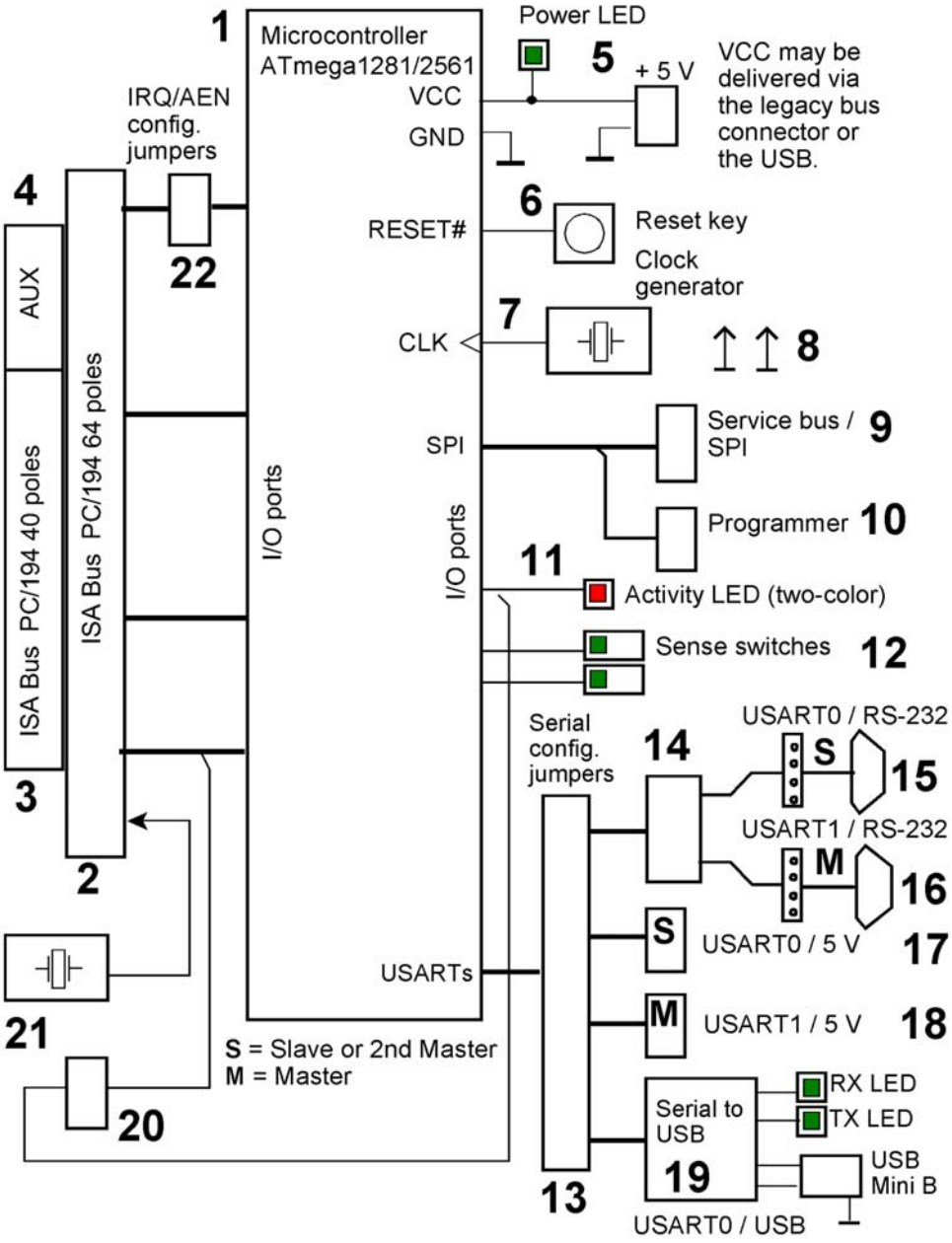

Microcontroller (1)
The board can be populated with an microcontroller Atmel ATmega 1281 or 2561 in a TQFP64 package. 128 or 256 kBytes Flash, 8 kBytes RAM, 4 kBytes EEPROM, maximum clock frequency 16 MHz.

PC/104 connector, 64 pins (XT bus) (2)
All ISA signals supported by the module are attached to this connector.

Note :
Details see below under "The ISA Bus" (page 7).

PC/104 connector, 40 pins (AT bus extension) (3)
The module does not support the AT bus. The purpose of this connector is only to provide 16-bit peripheral modules with static signal levels, indicating that 16-bit operation will be not supported. If no 16-bit modules are to be employed, the connector may be omitted.

Auxiliary connector, 8 or 12 pins (4)
This connector is only effective if the module is plugged onto the ISA baseboard 14a. An 8-pin or 12-pin connector can be fitted. 8 pins are used to supply the host controller. Contact assignment and physical position correspond to some kind of industry standard, to the additional connector of the so-called MOPS single board computers, manufactured by Kontron. The extension to 12 contacts is used to provide three additional address enable (AEN) signals to the slots of the baseboard (geographical addressing). 8-pin connectors may be available from appropriate manufacturers. 12-pin connectors must be manufactured purposefully (by sawing off an appropriate piece of a standard PC/104 connector).

Power supply terminal block and Power LED (5)
Power must be supplied from outside. The board has no voltage regulator and no anti-reversal protection. The operating voltage is 5 V. It can be supplied via the terminal block or any other connector with VCC and GND pins.

Notes:

1. The power supply via the USB connector does not comply with the USB standard. If attached to a USB host, this provision should be used only for testing, experimenting and the like.
2. Power supply devices with USB connectors can be used (e.g., chargers or so-called power banks). However, do not feed a larger ISA system via this connection, because PCB traces of the USB attachment cannot carry large currents. Current should not exceed approx. 800 mA.
3. If other modules attached to the ISA bus need other operating voltages, they must be supplied via the ISA bus connectors (2), (3) or the auxiliary connector (4).

Reset key (6)
The reset key is an inexpensive, but convenient means to facilitate debugging and troubleshooting.

Note:
Key actuation will reset only the microcontroller. To reset the bus devices, an ISA_RESET pulse must be generated by software.

Clock generator (7)
A complete crystal clock generator can be inserted. This allows to operate the microcontroller up to its maximum clock frequency. The nominal clock frequency is 16 MHz.

Ground test points (8)
Two ground test points can be inserted to support oscilloscope attachment and the like.

Service bus header (9)
The service bus comprises 8 signals. The service bus is composed of 4 bit-positions from port B and 4 bit-positions from port D. All bits are freely programmable. It can be employed to implement

an SPI interface (master or slave), accompanied by 4 additional signals (which can be used to select SPI peripherals or to trigger interrupts). The header comprises VCC and GND pins. They can be used to power external circuitry or to feed the module.

The service bus:

7	6	5	4	3	2	1	0
SRVBUS7	SRVBUS6	SRVBUS5	SRVBUS4	SRVBUS3	SRVBUS2	SRVBUS1	SRVBUS0
Port B3	Port B2	Port B1	Port B0	Port D7	Port D6	Port D5	Port D4
MISO	MOSI	SCK	SS#				

Programming header (10)
The pin assignment corresponds to that of the industry-standard Atmel programmers. The header comprises VCC and GND pins. They can be used to power external circuitry or to feed the module. The VCC rail connection is controlled via pin header JP1.

Activity LED (two-color) (11)
The activity LED can be controlled by two microcontroller signals, LED_A and LED_B. These signals are used to enable the Device Detection feature, too.

LED_A	**LED_B**	**Effect**
Low	Low	LED off
Low	High	LED lights green
High	Low	LED lights red
High	High	LED off. Device Detection enabled

Sense switches (12)
The on-off position of two switches can be sensed by two microcontroller signals, SENSE_SW1 and SENSE_SW2. These signals are low-active.

Serial interfaces configuration (13)
The serial interfaces are configured by jumpers via the pin headers JP5 to JP8.

Note :
Details of the serial interfaces configuration see below under "Serial Interfaces" (page 9) and "Configuring the ISA Host Adapter" (page 10).
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RS-232 level converter (14)
Level conversion is done by a MAX232 level converter IC.

USART0 RS-232 slave connectors (15)
The RS-232 signals belonging to USART0 are to be attached via pin headers o a 9-pole D-sub connector. The VCC and GND pins can be used to power external circuitry or to feed the module.

USART1 RS-232 connectors (16)
The RS-232 signals belonging to USART1 are to be attached via pin headers o a 9-pole D-sub connector. The VCC and GND pins can be used to power external circuitry or to feed the module.

USART0 5-V signalization header (17)
This header is connected to USART0. The header comprises VCC and GND pins. They can be used to power external circuitry or to feed the module. The serial signals are directly connected to the microcontroller.

USART1 5-V signalization header (18)
This header is connected to USART1. The header comprises VCC and GND pins. They can be used to power external circuitry or to feed the module. The serial signals are directly connected to the microcontroller.

Note:
The VCC rail connection in both headers (17), (18) is controlled via pin header JP6.

USB-to-serial converter (19)
USB-to-serial conversion is done by a FT232RL IC. The USB connector is of the Mini-B type. To facilitate troubleshooting, two LEDs are provided, indicating transmit and receive activities (TX LED, RX LED).

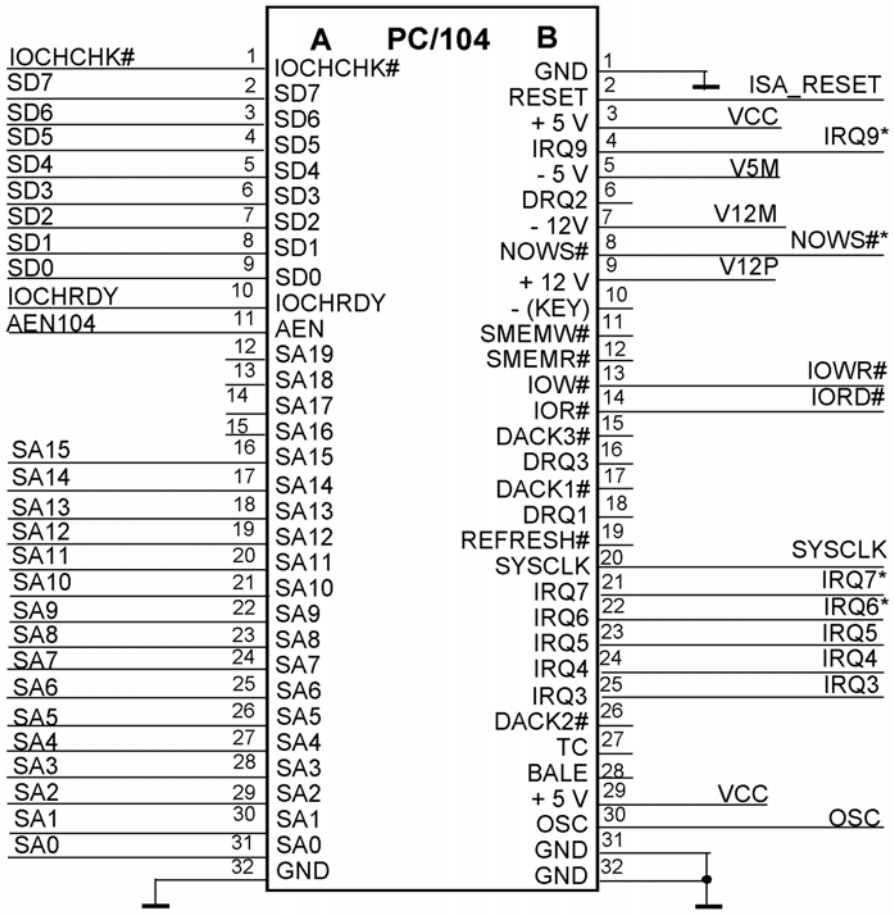
Device Detect feature (20)
This feature consists of a NAND gate and a resistor. Both LED signals (LED_a, LED_B) are used to control this feature. Details see below under "The Device Detect Feature" (page 13).

ISA OSC signal (21)
OSC is a general-purpose clock. It is not related to the ISA bus timing. The nominal frequency is 14,31818 MHz, the NTSC color burst frequency.

IRQ / AEN configuration (22)
The pin headers JP2, 3, and 4 allow configuring the microcontroller signals SEL_A, SEL_B, and SEL_C for different functions.

Microcontroller signal	1st function	2nd function
SEL_A	AEN2 on ISA baseboard 14a (output)	ISA IRQ6 (input)
SEL_B	AEN3 on ISA baseboard 14a (output)	ISA IRQ7 (input)
SEL_C	ISA NOWS# (input)	ISA IRQ9 (input)

The ISA Bus



*: Support of these signals is to be configured manually (jumpers).

ISA bus signals	Function	Notes
SD7...SD0	Data bus (8 bits)	The microcontroller may treat the SD signals as analog inputs
SA15...SA0	Address bus (16 bits)	I/O addressing only
AEN	Address Enable	Must be Low to enable I/O address detection. The microcontroller supports up to 4 AEN signals to facilitate geographic addressing (to be configured)
IOW#	I/O Write strobe	
IOR#	I/O Read strobe	
IOCHRDY	I/O Channel Ready	Low: wait state High: ready; no wait state
IOCHCHK#	I/O Channel Check	Device error signalization

ISA bus signals	Function	Notes
NOWS# (SRDY#)	No Wait State	Low: terminate the bus cycle immediately (fast cycle without wait states). To support this signal, configuration is required
ISA_RESET	Bus Reset	Resets all devices. Devices must tri-state all bus drivers
SYSCLK	System Clock	Bus clock. Most of the peripheral modules and cards work asynchronously, without regard to SYSCLK
OSC	Oscillator Clock	Uncommited clock signal. Some peripheral modules and cards use this signal as clock source
IRQ3, 4, 5	Interrupt signals	
IRQ6, 7, 9	Interrupt signals	To support these signals, configuration is required

Clock signals

The ISA specification stipulates two clock signals, the SYSCLK (BCLK) signal and the OSC signal. Frequencies and use are shown in Table 2. Most of the modules and cards make no use of the bus clock; they connect and respond to the bus asynchronously. However, some devices employ clock signals nevertheless, occasionally in a somewhat unexpected way. An example is an add-in card, which uses the OSC signal for clocking sequencers and counters.An OSC signal can be delivered by inserting a clock oscillator (21), a SYSCLK by programming the counter-timer unit 2A in the microcontroller.

Clock signal	Nominal frequency	Usage
SYSCLK (BCLK)	8 MHz (min. 6 MHz)	Bus clock. In the specifications, bus timing is related to SYSCLK. However, the bus is operated asynchronoulsly.
OSC	14,31818 MHz (70 ns period)	General-purpose. Occasionally used for clocking timers, sequencers and the like.

Table 1 The ISA bus comprises two clock signals. However, they are to be supported only if necessary.

Bus addressing vs. geographic addressing

The decisive bus signal is AEN (Address Enable). In I/O bus cycles, the address will be decoded only if AEN is de-asserted (Low). The PC/104 address enable signal is AEN104. Stacked modules see only this signal. The particular device must be selected by bus addressing.

The ISA baseboard 14a supports geographic addressing. Each bus slot can have its own AEN signal. Additional signals AEN1 to AEN3 are available on the baseboard via the (non-standard) auxiliary connector (4). AEN2 and AEN3 must be configured by jumper (pin headers JP2 and JP3).

Serial Interfaces

Two USARTs
The microcontroller provides two serial interface controllers, called Universal Synchronous and Asynchronous Receivers and Transmitters (USARTs).

Two modes – slave and master
Th serial interfaces can be employed to connect the module upstream to a host machine or downstream to attached devices. In upstream connection, the module is seen as Data Communications Equipment (DCE) and operated upon as a slave device. In downstream connection, the module acts as Data Terminal Equipment (DTE) and behaves as the master device.

Serial signalization
There are three flavors of serial signalization: the 5-V signalization, the RS-232 signalization and the USB signalization. At the USB, the module can act only as a device. Hence, the USB attachment is available only for slave operation at USART0.

USART 0	USART 1
Slave 5 V	Master 5 V
Slave RS-232	Master RS-232
Slave USB	
2nd Master 5 V	
2nd Master RS-232	

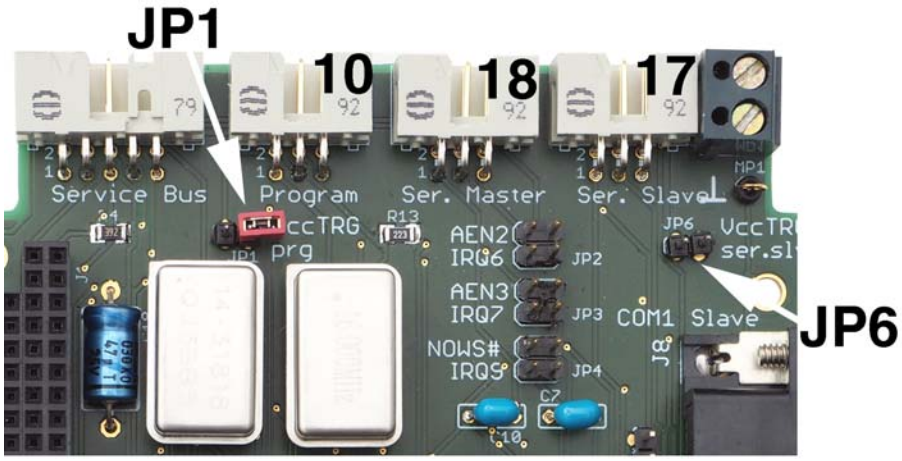
Interface	5-V connector		RS-232 pin header		RS-232 D-sub 9 connector		
	TX	RX	TX	RX	TX	RX	Gender
Slave	Pin 1	Pin 3	Pin 3	Pin 2	Pin 2	Pin 3	Female
Master	Pin 3	Pin 1	Pin 2	Pin 3	Pin 3	Pin 2	Male

Slave and master with regard to RS-232 signalization

- A Slave is a DCE device, like every RS-232 device downstream of a personal computer. The RS232-connector is a female DSub9 connector with TX on pin 2, RX on pin 3.
- A Master is a DTE device. The RS232-connector is a male DSub9 connector with TX on pin 3, RX on pin 2. If J8 is a female DSub9, an appropriate gender changer may be required.

Configuring the ISA Host Adapter

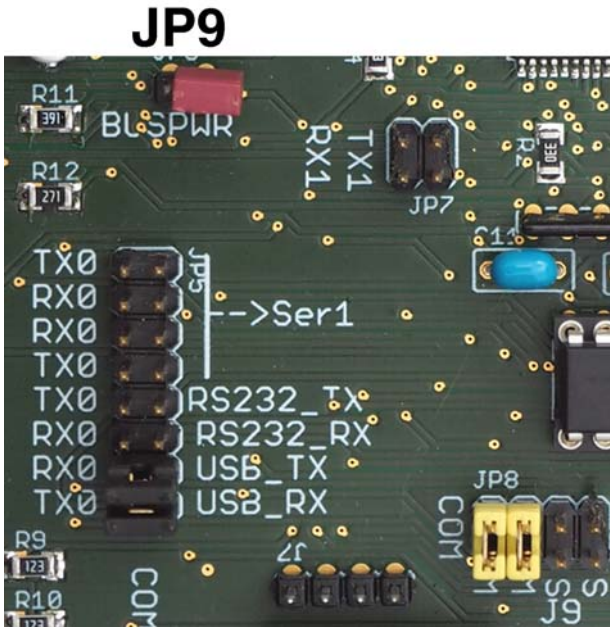
JP1 – VCC to programming header J1 (10)
Insert jumper JP1 to connect the programming header J1 (10) to VCC.



JP6 – VCC to 5-V serial headers J4 (17) and J5 (18)
Insert jumper JP6 to connect the 5-V serial headers to VCC.

JP9 – Power the module from the USB connector
Insert jumper JP9 if the module is to be powered by the USB.

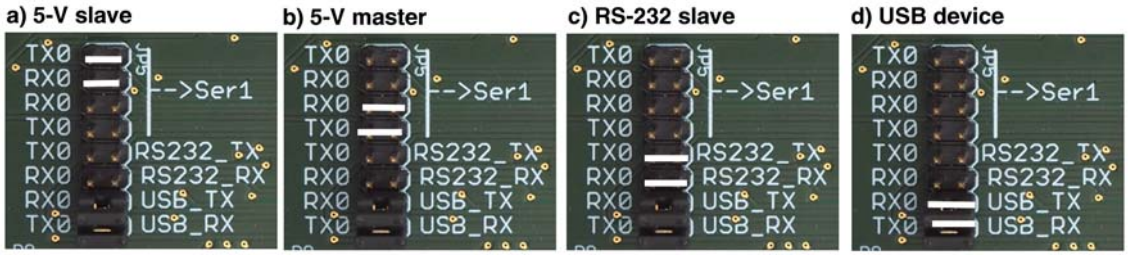
Note:
If the module is operated as a USB device (in contrast to attaching to a USB charger or power bank), this method of drawing power is not compliant with the USB standards. Use it only for bring-up and experimental purposes. In all cases, USB current should not exceed approx. 800 mA.



JP5 – USART0 configuration

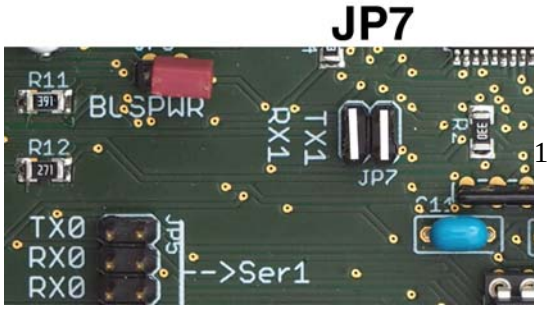
Insert two jumpers to connect the desired serial signals to USART0. One of the following configurations can be selected:

a) 5-V slave,
b) 5-V master (2nd master),
c) RS-232 slave,
d) USB device (slave).



JP7 – using USART1 with R2-232 signalization

If USART1 is to be configured for RS-232 signalization, insert two jumpers to connect the USART signals to the MAX232 level converter.



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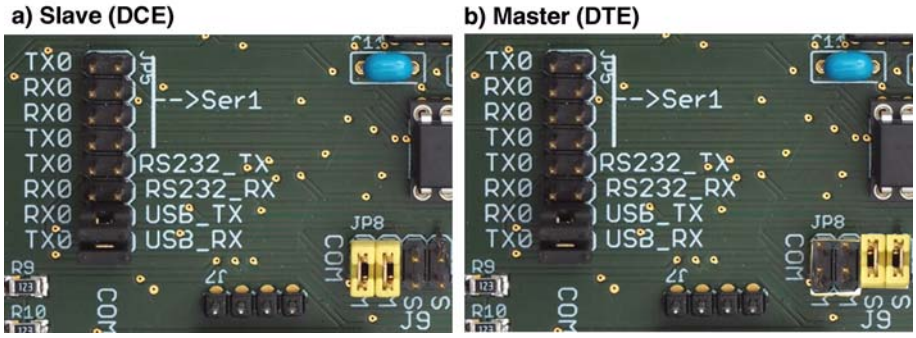
JP8 – configuring the RS-232 attachment of USART0

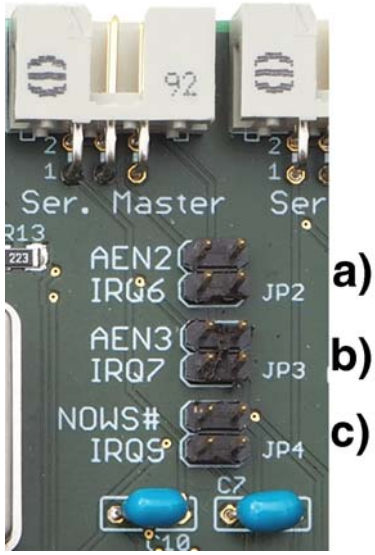
This interface can be operated in one of two modes. Insert two jumpers accordingly:

a) Slave or DCE. TX on pin 3, J6 and pin 2, J8. RX on pin 2, J6 and pin 3, J8.
b) Master or DTE. TX on pin 2, J6 and pin 3, J8. RX on pin 3, J6 and pin 2, J8.



JP 2, 3, 4 – configuring the signals SEL_A, SEL_B, and SEL_C
These microcontroller signals can be used for different purposes:

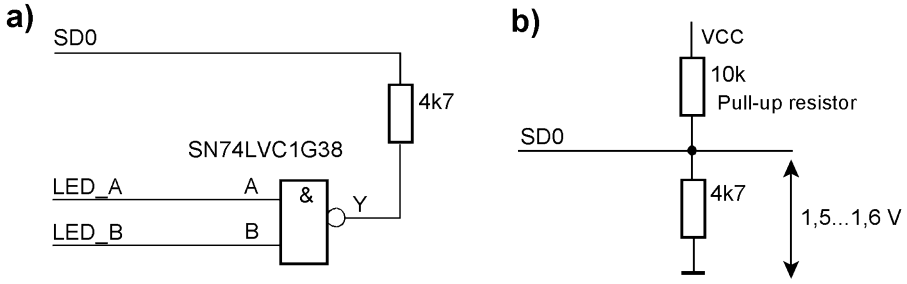
a) SEL_A can be programmed as an additional address enable signal AEN2, or to support the ISA interrupt signal IRQ6. Insert jumper JP2 accordingly.
b) SEL_B can be programmed as an additional address enable signal AEN3, or to support the ISA interrupt signal IRQ7. Insert jumper JP3 accordingly.
c) SEL_C can be programmed to support either the ISA signal NOWS#, or the ISA interrupt signal IRQ9. Insert jumper JP4 accordingly.



Note:
The address enable signals AEN2 and AEN3 are effective only on the ISA baseboard 14a. To connect these signals to the baseboard, the auxiliary connector (4) must be installed.

The Device Detect feature

The purpose is to find out which bus addresses are occupied by devices and which not. When a read (input) cycle is initiated and a device claims the bus address, data bus lines will be forced to a Low or High level. When no device reacts to the bus address, the data bus will not be driven. The different outcomes of a read cycle (Low, High or nothing) can be detected by analog-to-digital conversion. To facilitate detecting that the bus is driven, a voltage divider holds a bus line on an intermediate level (between Low and High).



The feature consists of a NAND gate and an additional resistor, supplementing the pull-up resistor of data bus signal SD0. The NAND gate is only a workaround, introduced because all microcontroller signals are used up for other purposes. So the LED signals are employed. The NAND gate will pull the resistor to ground level if both LED signals are High (a). Thus this resistor and the pull-up resistor of data signal SD0 constitute a voltage divider (b). During device detection, SD0 will be treated as an analog signal. A bus address will be emitted and a read cycle initiated. If no device claims the address, the signal level will be around 1,5 to 1,6 V. If a device responds, the signal level will be Low or High (less than 0,7 V or higher than 2 V). This way, all bus addresses can be scanned by software.

The Programming Interface

Port A

7	6	5	4	3	2	1	0
SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Output							

Port B = Connectors J2 und J6:

7	6	5	4	3	2	1	0
IOCHK#	IOCH RDY	ISA_ RESET	SYSCLK	SRVBUS 7	SRVBUS 6	SRVBUS 5	SRVBUS 4
		OC1A	OC2A	MISO	MOSI	SCK	SS#
Input	Input	Output	Output	Initialize service bus according to intended use			

Initialize unused service bus signals as inputs with internal pull-up's activated.

Port C

7	6	5	4	3	2	1	0
SA15	SA14	SA13	SA12	SA11	SA10	SA9	SA8
Output							

Port D

7	6	5	4	3	2	1	0
SRVBUS 3	SRVBUS 2	SRVBUS 1	SRVBUS 0	TX1	RX1	IRQ4	IRQ3
Initialize service bus according to intended use				Output	Input	Input	Input

Initialize unused service bus signals as inputs with internal pull-up's activated.

Port E

7	6	5	4	3	2	1	0
SEL_C	SEL_B	SEL_A	IRQ5	SENSE_S W2	SENSE_ SW1	TX0	RX0
				Input	Input	Output	Input

SEL_A = IRQ6 or AEN2 or unused
SEL_B = IRQ7 or AEN3 or unused
SEL_C = NOWS# or IRQ9 or unused
AENs are outputs. IRQs and NOWS# are inputs.
Initialize unused signals as inputs with internal pull-up's activated.

Port F

7	6	5	4	3	2	1	0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Bidirectional data bus / A/D converter inputs							

In idle state: inputs. Pull-up resistors will hold the signal at high level.

Port G

5	4	3	2	1	0
AEN1	AEN104	LED_B	LED_A	IORD#	IOWR#
Outputs					

AEN104 is the address enable signal in the PC/104 connector (2).
AEN1 is available on the ISA baseboard 14a via the auxiliary connector (4).